Improved Sense-Amplifier-Based Flip-Flop: Design and Measurements

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***Abstract*—Design and experimental evaluation of a new sense-amplifier-based flip-flop (SAFF) is presented. It was found that the main speed bottleneck of existing SAFF's is the cross-coupled set-reset (SR) latch in the output stage. The new flip-flop uses a new output stage latch topology that significantly reduces delay and improves driving capability. The performance of this flip-flop is verified by measurements on a test chip implemented in 0.18 μm effective channel length CMOS. Demonstrated speed places it among the fastest flip-flops used in the state-of-the-art processors. Measurement techniques employed in this work as well as the measurement set-up are discussed in this paper.**

***Index Terms*—CMOS digital integrated circuits, clocking, flip-flops, sense-amplifier.**

I. Introduction

A DIGITAL system can incorporate a variety of clocking schemes that impose constraints on the latching elements, thus determining how they are used in the system. The most commonly encountered schemes are single-phase and two-phase clocking. A detailed analysis of the timing requirements in synchronous digital systems is presented in the paper by Unger and Tan [1]. A comparative analysis of latches and flip-flops commonly used in high-performance systems today is presented in [3], [11]. This analysis deals with the trade-offs that are always possible between speed and power and the effect of the setup time on the cycle time of the system.

Timing elements, latches and flip-flops, are critical for the performance of digital systems because of the tight timing constraints and requirements for low power [12]–[22]. Loading of the clock distribution network is important because in high-performance systems power consumption attributed to the clock consumes 20%–45% of the total power consumed by the digital system [10]. Short setup and hold times are also essential for performance, but often overlooked. In a complex system it is very often necessary to have the ability to scan the data from the flip-flops in and out of the system during the test and diagnostic process. In addition, as the frequency of operation increases, the trend in reducing the number of logic levels between the pipeline stages requires that some portion of the logic be embedded into the flip-flop. Furthermore, the impact of the clock skew on the minimum cycle time increases in deep submicrometer designs as the clock skew does not follow the technology scaling. Thus the ability to absorb the clock skew without impact on setup time becomes important. These additional requirements imposed on latches and flip-flops are often given equal importance as to the performance features of the latching element itself.

The amount of cycle time taken out by the flip-flop consists of the sum of setup time and clock-to-output delay. Therefore, the true measure of the flip-flop delay is the time between the latest point of data arrival and corresponding output transition. Deeply pipelined systems exhibit inherent parallelism that requires higher fan-outs at the register outputs. This impacts the requirements for higher flip-flop driving strengths.

Recently reported flip-flops achieve small delay between the latest point of data arrival and output transition. Typical representatives are sense-amplifier-based flip-flop (SAFF) [7], hybrid-latch flip-flop (HLFF) [13] and semi-dynamic flip-flop (SDFF) [18], [20]. Hybrid flip-flops, HLFF and SDFF, outperform reported sense-amplifier-based designs, because the latter are limited by the implementation of their output latch [24].

In this paper, we present a newly developed SAFF, that overcomes the major shortcoming of the previously reported SAFF. In Section II, we present the analysis of the SAFF operation and discuss the drawbacks of the structure that has been commonly used [4]. Section III reviews the operation of the sense amplifier (SA) as a pulse-generating stage. The fourth section presents the design of the new latch in the second stage. Implementation of the new flip-flop, measurement setup and results are presented in Section V. Section VI presents the performance comparison with recently reported flip-flops, which is followed by a brief conclusion in Section VII.

II. Sense-Amplifier-Based Flip-Flop

A mechanism illustrating flip-flop operation is shown in Fig. 1. It is also essential to distinguish it from the master–slave (MS) latch combination consisting of two cascaded latches. MS latch pair can potentially be transparent if sufficient margin between the two clocking phases is not assured.

In general, a flip-flop consists of two blocks: a pulse generator (PG) and a slave latch (SL), similar to the MS latch combination consisting of master and slave latches. In the flip-flop structure, the first stage (PG) is a function of the clock and data signals. Therefore, as a result of changes in clock and data values a pulse

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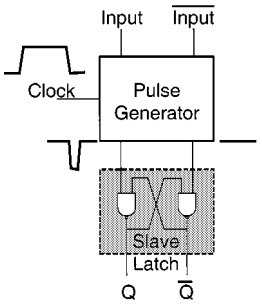

Fig. 1. General structure of a flip-flop.

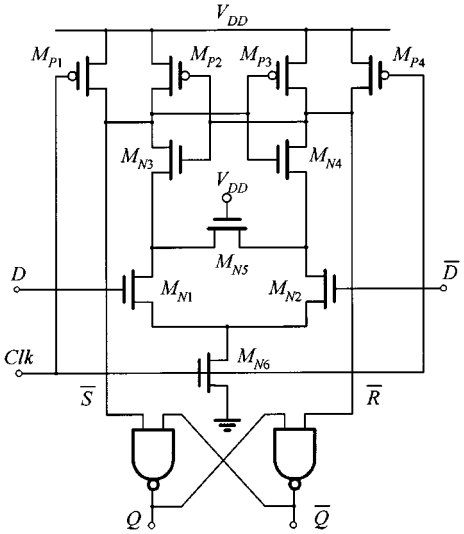

Fig. 2. SAFF [7].

of a sufficient duration is produced. This pulse in turn sets the slave latch. Depending on a particular realization, the PG stage is sensitive to the transition of the clock (from low-to-high, or high-to-low) and not to its level (as is the case with MS combination). This sensitivity in the implementation of the PG stage may pose a danger under certain conditions in terms of reliability and robustness of operation. Thus, the use of flip-flops has been prohibited in some design methodologies such as IBM's LSSD [22].

The SAFF consists of the SA in the first stage and the slave set-reset (SR) latch in the second stage as shown in Fig. 2, [7]. Thus SAFF is a flip-flop where the SA stage provides a negative pulse on one of the inputs to the slave latch: $\overline{S}$ or $\overline{R}$ (but not both), depending whether the output Q is to be set or reset.

The pulse-generating stage of this flip-flop is the SA described in [5], [6]. It senses the true and complementary differential inputs. The SA stage produces monotonic transitions from one to zero logic level on one of the outputs, following the leading clock edge. Any subsequent change of the data during the active clock interval will not affect the output of the SA. The SR latch captures the transition and holds the state until the next leading edge of the clock arrives. After the clock returns to inactive state, both outputs of the SA stage assume logic one value. Therefore, the whole structure acts as a flip-flop.

III. Review of the Pulse-Generating Stage Operation

When Clk is low, nodes labeled $\overline{S}$ and $\overline{R}$ are precharged through small M_{P1} and M_{P4} pMOS transistors, Fig. 2. The lower limit on the size of these transistors is determined by their capability to precharge the nodes in one half of the cycle. The high state of $\overline{S}$ and $\overline{R}$ keeps M_{N3} and M_{N4} on, charging their sources up to $V_{DD} - V_{tN}$ because there is no path to ground due to the off state of the clocked transistor M_{N6}. Since either M_{N1} or M_{N2} is on, the common node of M_{N1}, M_{N2}, and M_{N6} is also precharged to $V_{DD} - V_{tN}$. Therefore, prior to the leading clock edge, all the capacitances in the differential tree are precharged.

The SA stage is triggered on the leading edge of the clock. If D is high, node $\overline{S}$ is discharged through the path M_{N3}, M_{N1}, M_{N6}, turning M_{N4} off and M_{P3} on. If $\overline{D}$ is high, node $\overline{R}$ is discharged through the path M_{N4}, M_{N2}, M_{N6}, turning M_{N3} off and M_{P2} on. After this initial change, further changes of data inputs will not affect the state of the $\overline{S}$ and $\overline{R}$ nodes. The inputs are decoupled from the outputs of the SA forming the base for the flip-flop operation of the circuit.

The output of the SA, which is forced low at the leading edge of the clock, becomes floating low if the data changes during the high clock pulse. The additional transistor M_{N5} allows static operation, providing a path to ground even after the data is changed. This prevents the potential charging of the low output of the SA stage, due to the leakage currents. Those currents cannot be neglected in low-power designs where the V_t is lowered in order to boost the performance affected by the scaling of the supply voltage.

However, the additional transistor M_{N5} forces the whole differential tree to be precharged and discharged in every clock cycle, independent of the state of the data after the leading edge of the clock. The additional transistor M_{N5} is minimized, to prevent a significant increase in delay of the SA stage, due to the simultaneous discharging of both the direct path capacitive load and the load of the opposite branch.

This flip-flop has differential inputs and is suitable for use with differential and reduced swing logic. It uses single-phase clock, and has small clock load. Its first stage assures accurate timing, due to its SA topology, which is very important at high operating frequencies.

IV. Symmetric Slave Latch

The SR latch of the SAFF, shown in Fig. 2, operates as follows: input $\overline{S}$ is a set input and $\overline{R}$ is a reset input. The low level at both $\overline{S}$ and $\overline{R}$ node is not permitted and that is guaranteed by the SA stage. The low level at $\overline{S}$ sets the Q output to high, which in turn forces $\overline{Q}$ to low. Conversely, the low level at $\overline{R}$ sets the $\overline{Q}$ high, which in turn forces Q to low. Therefore, one of the output signals will always be delayed with respect to the other. The rising edge always occurs first, after one gate delay, and the falling edge occurs after two gate delays. Additionally, the delay of the true output, Q, depends on the load on the complementary output, $\overline{Q}$, and vice versa. This limits the performance of the SAFF.

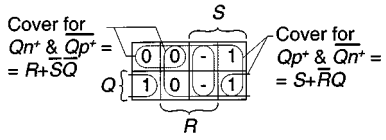

Fig. 3. Karnaugh map for Q^+ and $\overline{Q^+}$ and equations for resulting pull-up and pull-down transistor networks, labeled as Qn^+ and Qp^+.

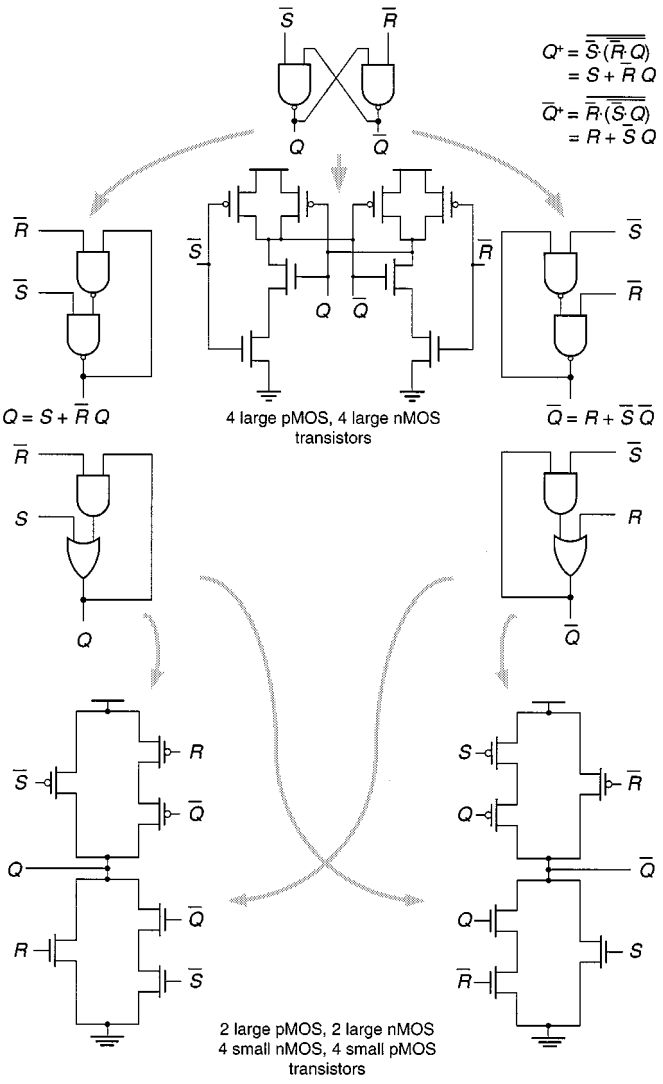

Fig. 4. Steps in obtaining new symmetric SL.

In order to overcome the problem of nonsymmetry of the SR latch in SAFF, we applied modifications to the SL stage. In the following description, Q represents a present, while Q^+ represents a future state of the SL, i.e., the state after the transition of the clock. The SL modification starts with logic representations for the new output values Q^+ and $\overline{Q^+}$ that are obtained by writing independent logic equations for the Q and $\overline{Q}$ outputs of the cross-coupled NAND gate SR latch.

$$Q^+ = S + \overline{R} \cdot Q \tag{1}$$

$$\overline{Q^+} = R + \overline{S} \cdot \overline{Q} \tag{2}$$

$Q^+ = S + \overline{R} \cdot Q$ is implemented as an AND-OR structure, where S is an OR branch of the circuit used to implement this

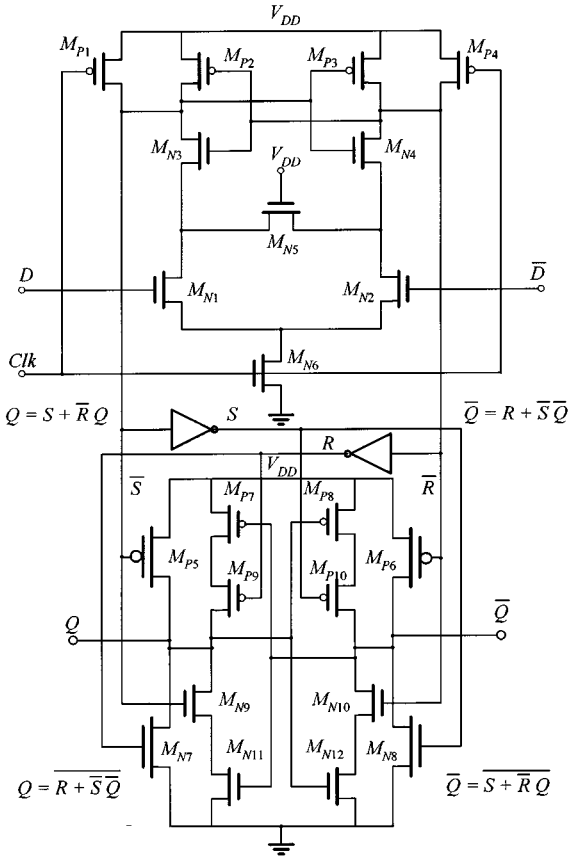

Fig. 5. Modified SAFF.

expression. Conversely, the same topology applies for the expression for: $\overline{Q^+} = R + \overline{S} \cdot \overline{Q}$. In this topology R signal is a parallel branch. The reason for choosing those expressions in implementing SL stage is to reduce the number of p-type series transistors in the branch responsible for the transition to one. This will be fully understood only when we analyze the entire SL stage resulting from these modifications.

Equations (1), (2) will be applied to the p-transistor networks of the corresponding cross-coupled NAND gates consisting the SL stage. The signals that are applied to the n-transistor networks are obtained by covering zeros on the corresponding Karnaugh maps for Q^+ and $\overline{Q^+}$. Symmetry of the two expressions is obtained by taking advantage of don't-care entries in the Karnaugh map for Q^+ and $\overline{Q^+}$. Therefore, we obtain the same circuits topology as the one resulting from (1), (2). This is illustrated in Fig. 3, representing the Karnaugh map for Q^+ and $\overline{Q^+}$ and the process of obtaining expressions for the n-type and p-type transistor networks in for Q^+ and $\overline{Q^+}$. The process of obtaining the new symmetric SL is illustrated in Fig. 4.

The resulting slave latch possesses the following features.

a. In the latch only one transistor in each branch is active when changing the state, thus allowing for small keeper transistors, as shown in Fig. 5.

b. The true and complementary trees of the new SL are symmetrical, resulting in equal delays of both outputs, Fig. 6.

Since the keeper transistors, M_{P7}-M_{P10} and M_{N9}-M_{N12}, are sized small, they quickly switch off during the transition. This allows outer, driver transistors, M_{P5}, M_{P6}, M_{N7}, and

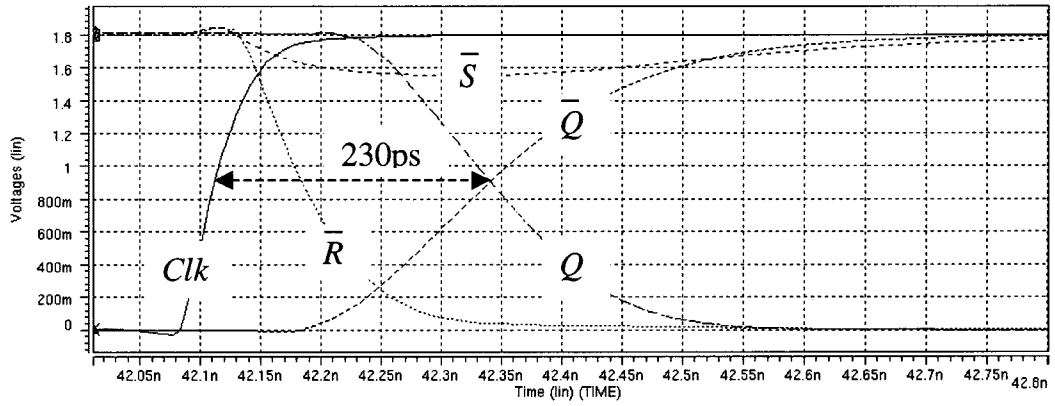

Fig. 6. Typical SAFF waveforms.

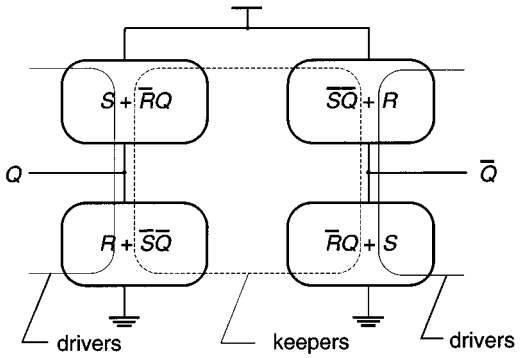

Fig. 7. Transistor functions in the new SL.

M_{N8}, to drive the load, and to change the state of the latch, as illustrated in Fig. 7. This feature makes output transistor size optimization a straightforward process. The only limit in minimization of keeper transistors is in the robustness of the output stage to the crosstalk during the low clock pulse.

In addition, only one transistor being active during the transition increases the driving capability of the output stage, and prevents the crow-bar current, reducing the power dissipation. Both true and complementary outputs have the same driving strengths, which is important not only for differential logic styles, but could also effectively double the driving capability of the flip-flop even when used with standard CMOS design. The self-loading at the output of the second stage is reduced as compared to a NAND implementation. The loading at the output with the NAND cross-coupled latch is two large gate capacitances and three large drain capacitances. The new output stage has loading of two small gates and two large and two small junctions.

The proposed SAFF, shown in Fig. 5, has all the advantages of earlier published SAFF's. It allows integration of the logic into the flip-flop, as well as reduced clock-swing operation [10]. The single-ended input version with multiplexed data scan and asynchronous reset is possible as shown in Fig. 8.

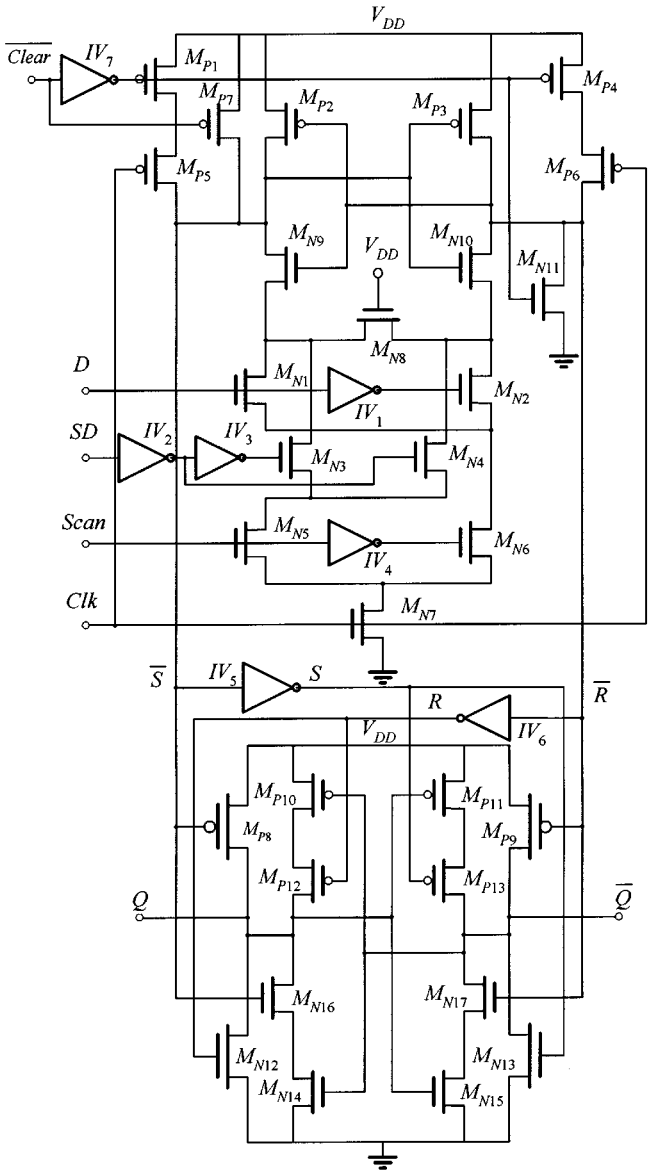

Fig. 8. SAFF with multiplexed scan and asynchronous reset.

V. Implementation and Measurements

The new SAFF is designed and implemented in 0.18 μm effective channel length CMOS technology. Transistor sizing is optimized using iterative procedure with the objective of achieving high speed and compact grid-based layout.

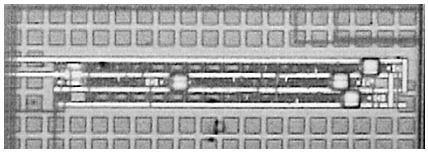

Fig. 9. Microphotograph of a test structure with probe pads.

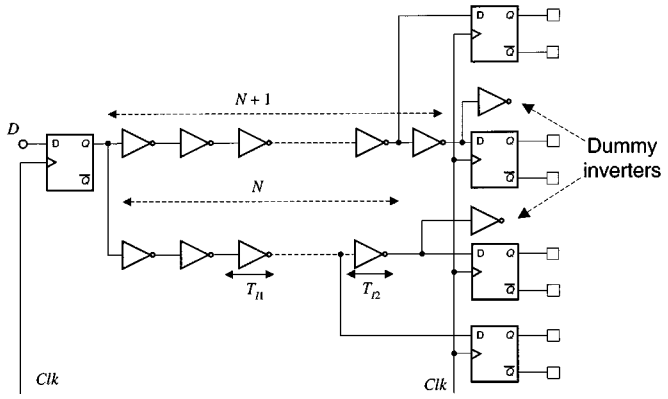

Fig. 10. Test structure implemented for measurements of flip-flop delay.

In order to measure the flip-flop performance, a simple test structure was implemented on the test chip shown in Fig. 9. The minimum delay between the latest point of data arrival and output transition is measured indirectly, using the structure from Fig. 10. Several chains of inverters as depicted in Fig. 10 were implemented. The measurement results were averaged over a set of sample chips obtained from the test run. The test chip contained a time-base generator, which allowed wide variation of clock frequency with resolution of 4 MHz. The clock frequency was raised until one of the flip-flops receiving signal from a chain of inverters failed. The time period corresponding to the failing clock frequency was calculated and entered into a set of equations describing the timing relationship between the flip-flop parameters and the signal delay. The clock frequency was changed in the 400–700 MHz range using an on-chip time-base generator.

The clock frequency was gradually increased until each of four paths fail to satisfy the setup timing, resulting in four periods, T_1, T_2, T_3, T_4. Those measurements are repeated for both rising and falling input data.

The inverter chain used in this measurement consisted of up to eight cells. Each cell consisted of three inverters with balanced high-to-low and low-to-high delays. This number of inverters in the chain was necessary in order to assure that the failure of all the flip-flops receiving the signal was occurring in the frequency range maintained by the time-base generator on the test chip. Equations (3)–(6) represent the timing relationship of the four paths used in this measurement, Fig. 10, where T_{I1} and T_{I2} are the cell delays. T_{I1} represents a cell delay with fan-out of one inverter and T_{I2} is the cell delay with fan-out of two. The inverter of the fan-out of two is actually loaded with one SAFF and one dummy inverter.

Each of the four register-to-register paths has a corresponding shortest cycle time:

$$T_1 = T_{Clk-Q} + T_{SU} + (N-1)T_{I1} + 2T_{I2} \quad (3)$$

$$T_2 = T_{Clk-Q} + T_{SU} + (N-1)T_{I1} + T_{I2} \quad (4)$$

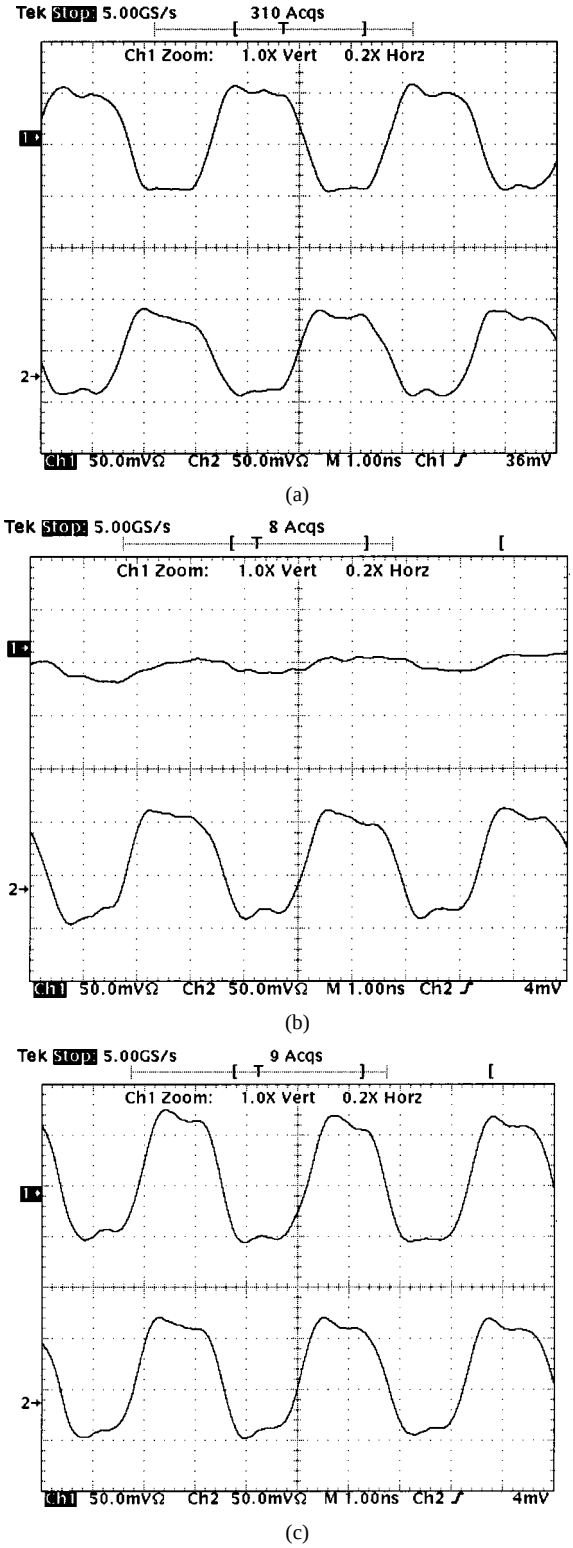

Fig. 11. Waveforms at the outputs of the two flip-flops preceded by chains of inverters differing in length by one. (a) Normal operation. (b) Sampling region. (c) Hold region.

$$T_3 = T_{Clk-Q} + T_{SU} + (N-2)T_{I1} + 2T_{I2} \quad (5)$$

$$T_4 = T_{Clk-Q} + T_{SU} + (N-2)T_{I1} + T_{I2}. \quad (6)$$

Since both the flip-flop and the inverter are designed to have the same rising and falling edge delays, the differences in high-to-low and low-to-high transitions are eliminated from (3)–(6).

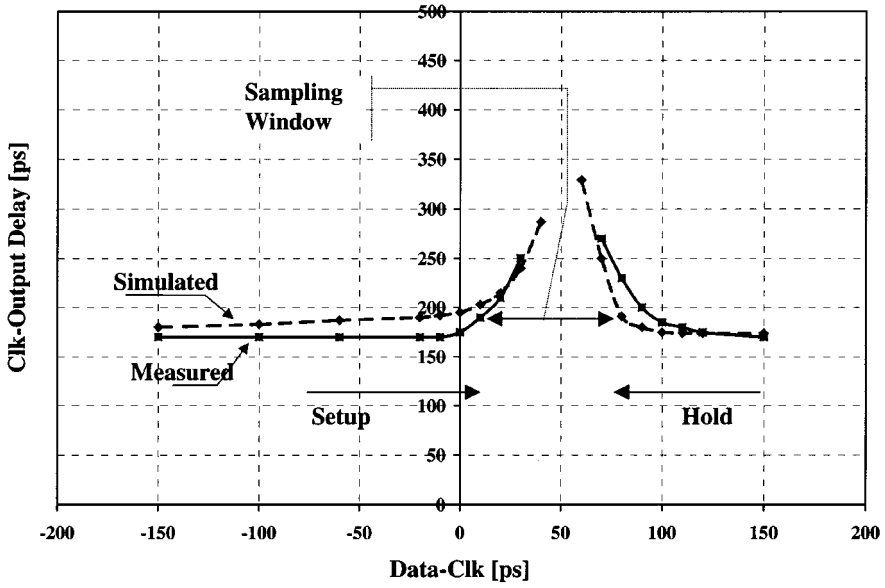

Fig. 12. Measured and simulated clock-to-output delay as a function setup and hold times.

TABLE I
SUMMARY OF SAFF PARAMETERS (NOMINAL PROCESS, POSTLAYOUT, $V_{DD} = 1.8$ V, $T = 25°$C, CLOCK AND DATA RISE TIMES 100 ps)

Parameter	Simulated, differential C_L = 200fF	Simulated, single-ended load = 2 inverters	Measured, single-ended load = 2 inverters
Rising delay, *Clk-Q*	230ps	165ps	170ps ± 20ps
Falling delay, *Clk-Q*	225ps	175ps	170ps ± 20ps
Setup time	-25ps	0ps	0ps ± 20ps
Hold time	160ps	90ps	80ps ± 20ps
Avg. Power	31μW	29μW	N.A.

By observing the differences in outputs between the pairs of flip-flops, the unknown values of inverter delays, T_{I1} and T_{I2}, and sums of setup time and Clk-Q delays can be measured.

At cycle times which are long enough for both flip-flops to successfully capture the data, the output waveforms at two flip-flops following the chains that differ in one inversion are out of phase as expected from Fig. 10, and shown in Fig. 11(a). As the clock frequency increases, the flip-flop that follows the longer inverter chain fails to capture the data due to setup violation, as observed in Fig. 11(b). With further shortening of the clock cycle the signal propagating through the longer inverter chain does not arrive in time, however, the flip-flop will at some point start to successfully capture the pervious value of the signal. The capturing of that previous signal value by the flip-flop will be stabilized only after the signal arrives after the hold-time window of the flip-flop, thus avoiding the hold-time violation. Capturing of the previous value of the data produces the same waveform as the output of the flip-flop receiving inverter chain path containing one inversion less, as shown in Fig. 11(c).

The problem of precise measurement of the setup and hold-time lies in the fact that the flip-flop delay increases as the signal approaches the point of setup and hold-time violation until the flip-flops fails to capture the correct data [2]. This change in Clk-Q delay is plotted in Fig. 12. Thus the precise setup and hold time delay measurements were done by observing the relative difference between the two flip-flop outputs following the inverter chains of different lengths. To assure that the relative difference in delay is attributed only to a setup (or hold) time violation the observing flip-flops were connected to the chains differing for a sufficient number of inverters, thus assuring that the flip-flop connected to the shorter path is far away from setup (or hold) violation. This makes the delay of the flip-flop connected to the shorter path constant and independent of the signal arrival time, thus attributing the difference in delay only to the setup (or hold) time dependency of the flip-flop under observation. In this measurement the clock signal divided by 16 is used as the data input, D and the degradation in Clk-Q delay is plotted versus the clock period. Fig. 12 shows simulated and measured clock-to-output delays as a function of setup and hold time.

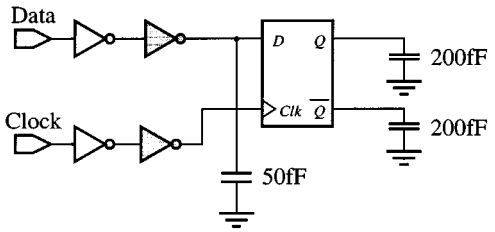

Fig. 13. Test bench for flip-flop comparison.

Simulated flip-flop waveforms (shown in Fig. 6) demonstrate the symmetry of true and complementary delays, even when driving 200 fF loads. The balance between the rising and falling transitions can be held over a wide range of output loads. Proposed SAFF shows very narrow sampling window of less than 100 ps. Sampling window is defined as the time interval in which the flip-flop samples the data value. During this interval any change of data is prohibited in order to assure robust and

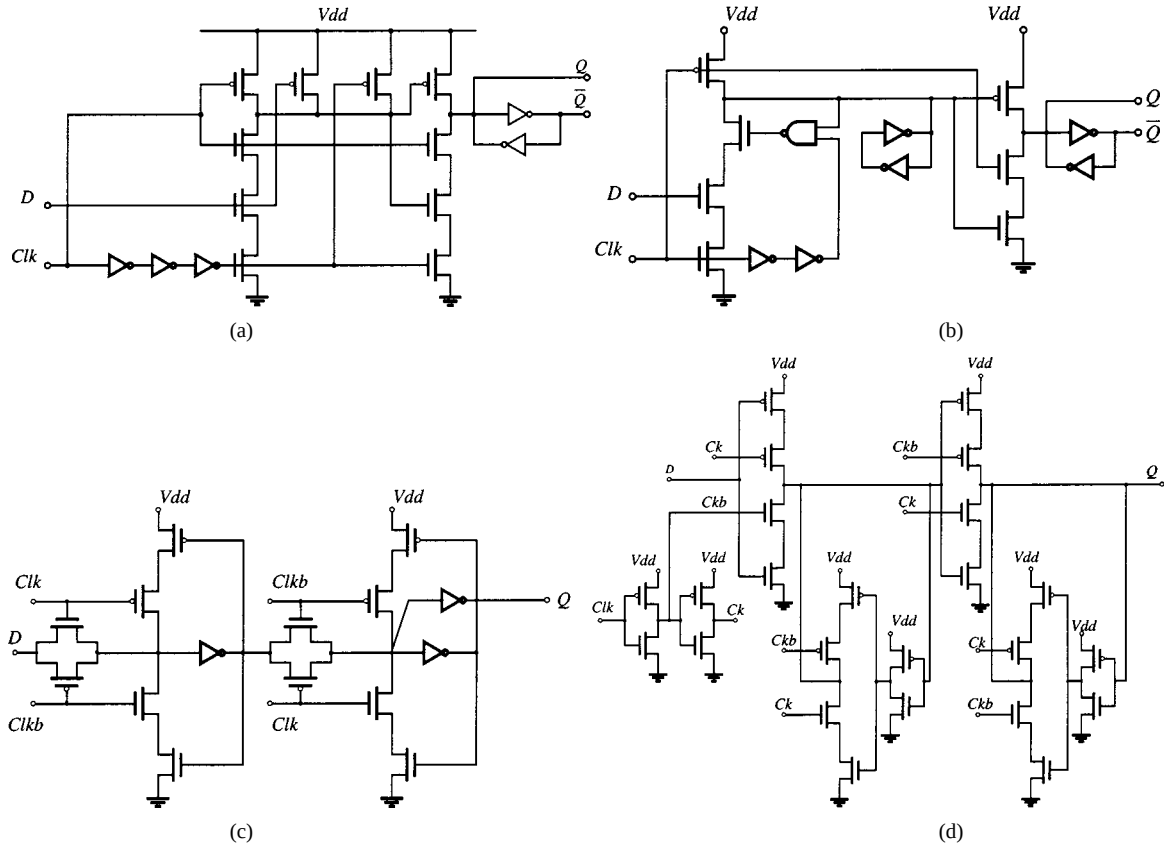

Fig. 14. Representative flip-flops. (a) Hybrid latch - flip-flop. (b) Semi-dynamic flip-flop. (c) TG MS flip-flop. (d) C^{2}MOS MS flip-flop.

reliable operation. We found that the hold time is dependent on the slope of the input signal. Thus it was possible to shorten the hold time, by buffering the data, as it was done in our scan path design, shown in Fig. 8.

Simulated and measured data is summarized in Table I. The measured results show a very good agreement with the simulation, which testifies not only to the accuracy of the post-layout simulation but a validity of described method for measuring flip-flop parameters as well. The accuracy of our measurement lies within ± 10 ps in both x and y directions.

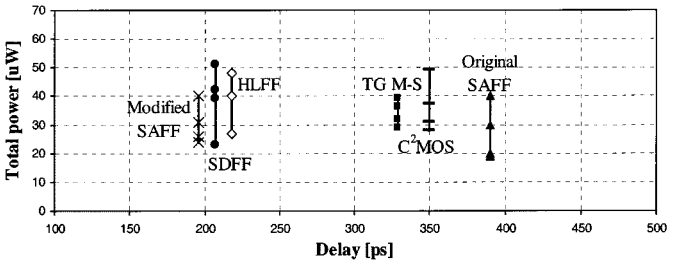

Fig. 15. Comparison of delays and power between different flip-flops.

VI. Comparison with Related Flip-Flops

The interest in high-speed flip-flop design re-emerged recently as the frequencies of operation passed 1 GHz. The importance of a good flip-flop design affects the power consumed by the clock as well as the available time in ever-shrinking pipeline. Many new latch and flip-flop architectures were published [4], [7]–[9], [12]–[21]. They demonstrated improvements in speed, power, reliability, clock load, setup and hold times. Flip-flop performance comparison with respect to speed and power dissipation in this work is done resembling the setup in [3], [11], with the test bench shown in Fig. 13.

In comparison to other recently published flip-flops, HLFF [13], Fig. 14(a), SDFF, Fig. 14(b) [18]–[20] modified SA flip-flop has the shortest delay, represented by the sum of setup time and clock to output delay. Transmission-gate MS latch pair (TG MS), Fig. 14(c), [12], and C^{2}MOS MS latch pair, Fig. 14(d), [23] are also used in comparison. The simulations were performed using BSIM 3v3 CMOS transistor model. Nominal process corner was used with $T = 25\ ^\circ$C and supply voltage of 1.8 V. All inputs were driven by large buffers, resulting in 100 ps, 20%–80% rise and fall times and outputs were loaded with 200 fF. All the flip-flops were optimized for minimum delay with output transistor sizes limited. Power consumption in Fig. 15 is shown for maximum, average, and minimum activities of the data input.

Table II shows the total gate length of all compared flip-flops, as an area estimate. The improved SAFF is about 20% larger than SDFF and HLFF, with a 5%–10% increase in speed, but features differential outputs, that both can drive the loads. The SAFF size can be reduced by about 5%, with small increase in speed if only one output is used.

VII. Conclusion

We developed, fabricated and tested an improved SA flip-flop. We presented a systematic method for its derivation, which allows flip-flop realization in a circuit topology yielding op-

TABLE II
TOTAL TRANSISTOR GATE WIDTH AS A MEASURE OF SIZE OF COMPARED FLIP-FLOPS

Flip-flop	New SAFF	SDFF	HLFF	TG M-S	C^2MOS	NAND-based SAFF
Total gate width [μm]	64	49	54	52	80	60

timal speed and power. The strong driving capability of this flip-flop makes it suitable for GHz design characterized with a short pipeline and high fan-out. The differential input signal nature of the flip-flop makes it compatible with the logic utilizing reduced signal swing. Further, we developed a method for accurate measurement of flip-flop parameters from the test chip. We obtained very good measurement accuracy of ± 10 ps under difficult conditions characterized with high test frequency. This flip-flop was implemented on a test chip in 0.18 μ CMOS technology. The measurement results place it on the top in terms of speed as compared to other flip-flops used in high-performance processors.

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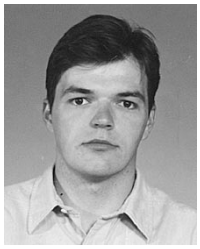

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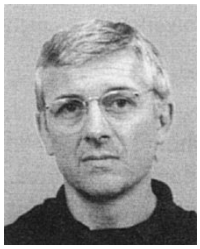

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