

# Low-Loss Polysilicon Waveguides Suitable for Integration within a High-Volume Electronics Process

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**Abstract:** Polysilicon waveguides are fabricated in a 300 mm wafer process representative of a complete high-volume electronic memory process. 6.2 dB/cm end-of-line loss is measured for narrow waveguides with a confinement factor scaling of  $5.1 \text{ cm}^{-1}$ .

**OCIS codes:** (230.7370) Waveguides; (220.4000) Microstructure fabrication; (250.5300) Photonic integrated circuits

## 1. Introduction and background

Low propagation loss deposited waveguides are an important component to enable photonic integration in the majority of high-volume electronics processes. Polycrystalline silicon waveguides are desirable in this role as propagation losses below 10 dB/cm are achievable [1,2,3] using materials already common in such processes. Additionally, the high index-contrast of poly-Si to silicon dioxide enables small bend radii passive photonic devices while well developed doping and contact processes enable active device fabrication [4]. However, previous demonstrations of low-loss poly-Si waveguides have utilized layer thicknesses of 200 nm or greater and reduced index-contrast oxynitride claddings to achieve such results. Further, the low-loss performance was not verified to withstand the high-temperature steps present in electronics processes. In this work, we present thin, high-index-contrast poly-Si waveguides fabricated in a complete 300 mm wafer process representative of state-of-the-art memory processes with end-of-line waveguide losses below 10 dB/cm for the first time.

An important constraint of process integration within electronics processes is an upper limit on the thickness of new layers that may be inserted into the existing material stack-up. For integration within the front-end of modern processes, this maximum layer thickness is often in the range of 150 to 200 nm. This constraint is set by a planarized fabrication process that requires thin layers to avoid high aspect ratios for small feature sizes. For such thin-core waveguides, the magnitude and correlation length of the top surface roughness may have a large impact on the modal propagation loss. This effect is pronounced in polycrystalline material where the grain structure may cause significant surface topology. As such, although prior work demonstrated 6.5 dB/cm for a 250 nm core thickness, similar waveguides showed double the propagation loss at 150 nm core thickness [2]. The next major constraint imposed by process integration is that the subsequent high-temperature steps in the process modify the properties of the deposited layer. Since the thermal processing can cause grain growth, the surface roughness, and therefore waveguide loss, may increase from the as-deposited film to end of line. Our previous work on 80 nm thick as-deposited CMOS poly-Si waveguides demonstrated 10 dB/cm waveguide loss [3] while end-of-line waveguides of similarly deposited films demonstrated five-fold higher losses of 55-65 dB/cm [4]. Finally, since the optical mode is confined not only in the waveguide core but also in the low-index cladding layers, the surrounding dielectric stack-up of the waveguide under test must be representative of the intended integration process.

## 2. Results and discussion

To provide a suitable process integration test platform, 120 nm thick poly-Si waveguides were deposited and patterned on 300 mm wafers within the surrounding dielectric stack-up representative of the state-of-the-art memory process. To measure the impact of the thermal processing, the wafers were split with and without the all of the high-temperature anneals present in the full process. To minimize the impact of this thermal processing on top surface roughness, the waveguide core was first deposited at low-temperature by LPCVD to form an amorphous film. Next, it was crystallized to form poly-Si with a  $\sim 950 \text{ }^\circ\text{C}$  anneal for 20 seconds in a nitrogen atmosphere. The roughness of the top surface of the poly-Si layer was measured by AFM to be 0.33 nm RMS with a 17.6 nm correlation length. This smooth surface is expected to contribute roughly 0.3 dB/cm loss from theoretical modeling [5].

To measure the resulting waveguide loss, “paperclip” structures (Fig. 1) were patterned in which straight waveguide sections of varying propagation lengths are connected by identical input and output bends and vertical grating couplers. To study the loss as a function of waveguide width, tapers are used to vary the width of the straight sections while keeping the width of the bending regions constant to avoid bending loss and higher-order-mode excitation. Fitting the slope of the total transmission loss to the change in straight section length therefore is a

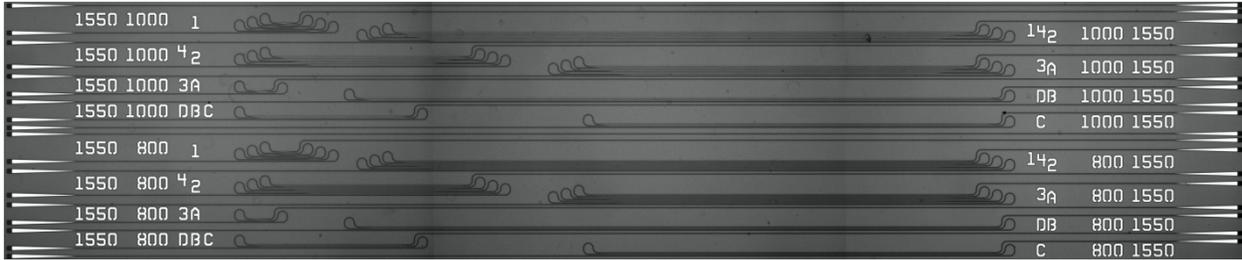


Fig. 1. Optical micrograph of “paperclip” waveguide loss test structures for two waveguide widths. Four differential lengths are used to measure propagation losses in with two different total length test structures designed for high and low loss cases. Width of micrograph region is 4 mm.

measure of the propagation loss as in the cutback measurement technique. The resulting losses at 1550 nm as a function of waveguide width for wafers with and without thermal processing are shown in Fig. 2a. The propagation loss was also measured at 1460 nm and 1280 nm for the thermally processed wafers and is shown in Fig. 2b. Due to the thin waveguide geometry and polarizing nature of the vertical grating couplers, the waveguides are only designed and measured for transverse-electric polarized light.

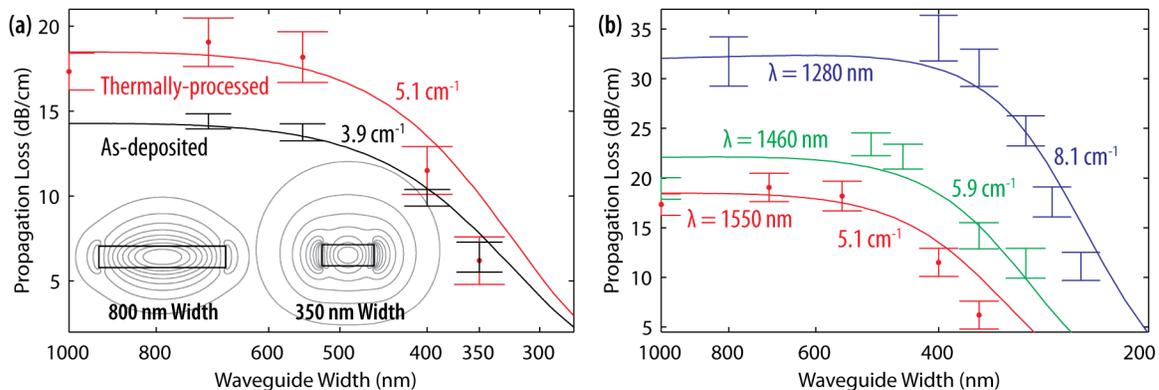


Fig. 2. (a) Propagation loss as a function of waveguide width for wafers with and without thermal processing representative of the full electronics process. Solid fit lines estimating the confinement factor scaling for the indicated bulk material losses overlay measured data points. Inset of electric field contours show confinement change from core to cladding material for narrow waveguide widths. (b) Propagation loss as a function of wavelength and waveguide width for the thermally processed wafer.

Although the waveguide loss increases slightly after thermal processing, both the as-deposited and end-of-line waveguide losses are below 10 dB/cm for 350 nm waveguide widths at 1550 nm. This increase can be attributed to an increase in surface roughness, but is well below the five-fold increase observed previously. The loss dependence on waveguide width qualitatively fits with a confinement factor scaling with the core material loss as shown in Figure 2. The narrow waveguides therefore enable long-distance, on-chip routing to be enabled with 6.2 dB/cm loss. For resonant devices and curves requiring tight bend radii, the increased confinement of the wider waveguides is required. For a maximally-confined singlemode width of 550 nm, the measured end-of-line waveguide loss is 18.2 dB/cm. This loss is sufficient to realize a resonant quality factor of 71,000. The bulk material loss may be attributed to the electronic state absorption within the polysilicon material or scattering off grain boundaries. Either physical origin may explain this scaling combined by the increase of loss at shorter wavelengths as shown in Fig. 2b. Further optimization of polysilicon deposition and anneal conditions may improve this result [1].

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