photonics integration scheme and to evaluate its feasibility by quantifying critical photonic device performance parameters. The dimensional precision demonstrated indirectly through optical measurements of the filter banks, combined with the potential of ultra-low-power wavelength locking, provides the basis for a scalable nanophotonics-electronics integration platform. Since the waveguide polysilicon layer is also the transistor gate and local interconnect layer of the standard bulk-CMOS process, available doping and metallization steps allow active devices such as carrier-injection modulators to be built upon this foundation [6]. On the detection side of the link, deeply-scaled CMOS processes already include a silicon-germanium layer for stress engineering the p-type transistor [51]. This lower bandgap layer may then be leveraged to integrate front-end photodiodes and form a complete photonic device platform at short operating wavelengths such as 1.2 μm where the SiGe alloy ratio provides a sufficient absorption coefficient. Since this platform is built into a state-of-the-art CMOS process, a major step in electronic-photonic circuit integration is enabled. The existing electronic CMOS infrastructure already demonstrated to fabricate 2 billion transistor circuits with high yield [52] could now be used to simultaneously fabricate nanophotonic circuits with high yield as well. By complying with all in-foundry processes, no further infrastructure investment is required. Additionally, sharing the mask costs and all wafer-level processing on multi-project wafer runs with the large number of electronics industry projects significantly lowers the incremental cost of developing systems and devices [23]. This work may also be carried over to thin-SOI-CMOS foundries where there is the potential of low-loss waveguides to enable further system applications.

Acknowledgements

The authors acknowledge Dr. Jagdeep Shah of DARPA for funding under contract numbers W911NF-06-1-0449 and W911NF-08-1-0362. The authors also acknowledge J. L. Hoyt and M. Schmidt of MIT for discussing the localized substrate removal method as well as D. Buss, S. Yu and R. Khamankar of Texas Instruments for discussing relevant CMOS processing steps. M. Georges, J. Leu and B. Moss of MIT designed the electronic circuits contained on the die shown in Fig. 1a.

#134664 - $15.00 USD Received 8 Sep 2010; revised 14 Oct 2010; accepted 18 Oct 2010; published 24 Jan 2011