Low Loss Waveguide Integration within a Thin-SOI CMOS Foundry

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***Abstract*—By requiring zero process changes and by complying with established electronic circuit design rules, photonic devices formed with 3dB/cm waveguides were fabricated alongside transistors achieving 4ps stage delay in a 45nm thin-SOI CMOS foundry.**

Keywords- CMOS process; optical waveguides

I. INTRODUCTION

Standardized fabrication of microchips with silicon photonic devices and circuits in multi-user fabrication facilities, known as foundries, promises to dramatically increase the pace of technology innovation in ways analogous to the late 20th-century transformation of the CMOS electronics industry [1]. Recently, photonics-only mask-shared fabrication runs have greatly increased access to advanced processing technology [2]. Integration of photonics with electronic circuits, however, has not provided widespread technology access or achieved monolithic integration of high-performance electronic and photonic devices. Past advances using proprietary facilities have utilized older CMOS technology to enable process modification [3] or achieved limited photonics performance [4]. This paper presents photonic devices with 3dB/cm waveguide loss fabricated in a 45nm thin-SOI CMOS foundry process with transistors achieving 4ps stage delay.

II. STANDARD PROCESS INTEGRATION

The 3-million transistor, 2.9 mm x 2.9 mm chip was fabricated in a multi-user run of the IBM 45nm transistor gate length silicon-on-insulator (SOI) CMOS foundry process, known by the technology identifier 12SOI [5]. Since the in-foundry processing follows a standard recipe, photonic integration must require zero in-foundry process changes.

This work was funded by DARPA award W911NF-10-1-0412, and also in part by the NSF, the FCRP IFC, MIT CICS, and the Trusted Foundry. The views expressed are those of the authors and do not reflect the official policy or position of the Department of Defense or the U.S. Government.

Design preparation was performed in Cadence Virtuoso and Encounter tools to enable electronic-photonic integration and compliant design submission [6]. Local pattern density on all relevant design layers were maintained in mask design while excluding optically-lossy metals from a 2-3 μm region around the waveguides. Custom auto-fill routines inserted 0.8μm x 0.8μm high density cells surrounding the photonic region where required to ensure process compliance. Several waivers for violations of standard process design rules were obtained through the standard foundry infrastructure. Most resulted from photonic devices being erroneously flagged during the automated design rule check processing as improperly formed electronic devices. Geometry waivers for the small, nanometer-scale notches formed by the curve discretization were also obtained, as these shapes have been shown to present no structural threat to process yield.

Since the thin-SOI CMOS electronics process is optimized for transistor performance and low thermal impedance, the buried oxide (BOX) layer that separates the silicon layer from the handle wafer is thinner than 200 nm, while 2-3 μm is common for photonics SOI wafers. The as-fabricated wafers therefore do not provide sufficient low-index cladding thickness underneath the silicon waveguide core to eliminate substrate leakage loss. Post-processing that can locally remove the underlying silicon has been demonstrated previously for photonics [4] and MEMS [7] applications. For faster characterization turnaround, in this work we instead use a substrate-transfer process by first mounting the die pad-side down to an oxidized silicon wafer. The silicon substrate of the die is removed using XeF_2 gas. Next, a thermally and electrically conductive replacement substrate of 6H-SiC is bonded to the CMOS layer stack using Norland Optical Adhesive 71 and the transferred die is released from the oxidized silicon handle wafer.

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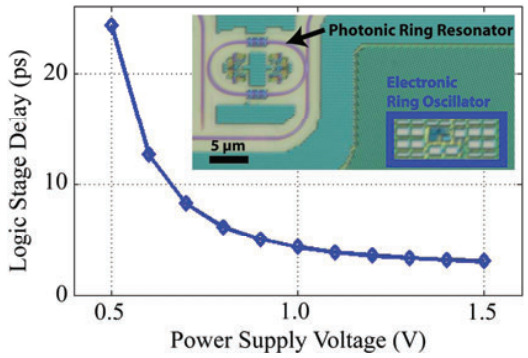

Figure 1. Stage delay of ring oscillator shown in micrograph inset.

III. Verification of Transistor Functionality

Electronic ring oscillators, placed in the photonic integration regions, indicate no observable transistor performance degradation verifying that photonic devices can be integrated in close vicinity to high-performance transistors. The logic stage delay characterized by the oscillator resonant frequency is shown in Fig. 1. The achieved switching time of less than 5ps is the fastest demonstration of transistor performance for a monolithically integrated photonic platform. The oscillator resonance frequency was remeasured after all post-processing was completed. The before and after measurements differ by less than 5% for all measured supply voltages. Similar electronic functionality studies have been performed for localized substrate removal processes as well [7].

IV. Waveguide Characterization

To be an enabling technology for a broad range of photonics applications, the integrated waveguide loss must be comparable to the best available silicon photonics results using photolithography that are in the range of 2 dB/cm for strongly confined modes [8]. In the SOI-CMOS process, the single-crystalline silicon layer that forms the transistor floating body may be patterned to form a waveguide. This is in contrast to the previous zero-change integration work in bulk-CMOS [4], where the polysilicon transistor gate was used. Strongly-confined waveguide propagation loss is measured to be approximately 3 dB/cm near 1310nm as well as near 1550nm as shown in Fig. 2a-b. Extracted intrinsic quality factors of 227,000 and 112,000 were obtained for 1280nm and 1550nm rings respectively as shown in Fig. 2c-d.

V. Conclusion

The electronic-photonic platform demonstrated in this work is an accessible, low-cost utilization of the existing electronics infrastructure to fabricate high-performance photonic devices alongside state-of-the-art CMOS transistors. Excellent passive photonic performance achievable with no in-foundry changes and simple post-processing using the thin-SOI-CMOS process removes the waveguide loss and transistor performance bottlenecks.

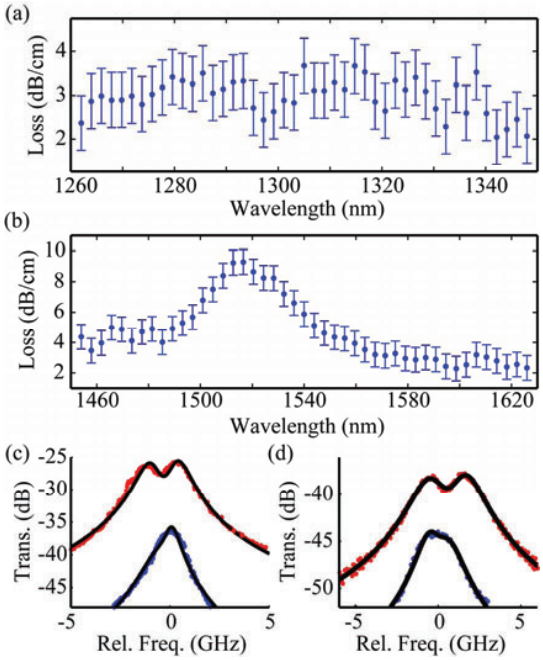

Figure 2. Propagation losses for single-mode waveguides measured near 1310nm (a) and 1550nm (b) using 4.1mm differential length structures. Measured fit transmission for drop ports of moderately-coupled (red points) and weakly-coupled (blue points) 20 μm radius rings at 1280nm (c) and 1550nm (d).

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