Table 1. Summary of experimentally measured waveguide losses, bulk absorption calculations and electric field overlaps with surfaces where roughness is a concern. Surface overlaps were calculated by integrating the electric field within 5 nm of each surface. All data presented is for λ = 1550 nm.

was obtained from the wide widths, the bulk loss extraction underestimates the loss of the 550 nm wide waveguide widths where the sidewall electric field overlap is an order of magnitude higher.

4. Conclusion

In this work, end-of-line polysilicon waveguides suitable for high-volume product integration have been demonstrated with propagation losses below 10 dB/cm for the first time. Low surface roughness enabled film thickness scaling below 200 nm with relatively low propagation loss increases. Characterizing the waveguide loss as a function of wavelength over a broad spectral region of technological interest enabled the dominant physical source of the loss to be identified as defect state absorption. Confinement factor scaling of the optical mode, which demonstrates the minimal effect of both top surface and line-edge roughness, enabled waveguide propagation losses of 6-15 dB/cm across this spectrum. These results have been achieved by optimizing the anneal conditions of the existing polysilicon transistor gate layer to minimize process complexity. This may enable a lower total system cost to the SPE approach that has achieved similar optical performance at 1550 nm [18]. By having performed this test in an emulation environment to eliminate road blocks to end product integration, it is now possible to explore next-generation memory systems that utilize this integrated photonic platform [3].

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