

# Photonic integration in a commercial scaled bulk-CMOS process

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**Abstract:** We demonstrate the first photonic chip designed for a commercial bulk CMOS process (65 nm-node) using standard process layers combined with post-processing, enabling dense photonic integration with high-performance microprocessor electronics.

**Keywords:** Silicon photonics, CMOS, add/drop filter, microring resonator, photonic integrated circuits

## Introduction

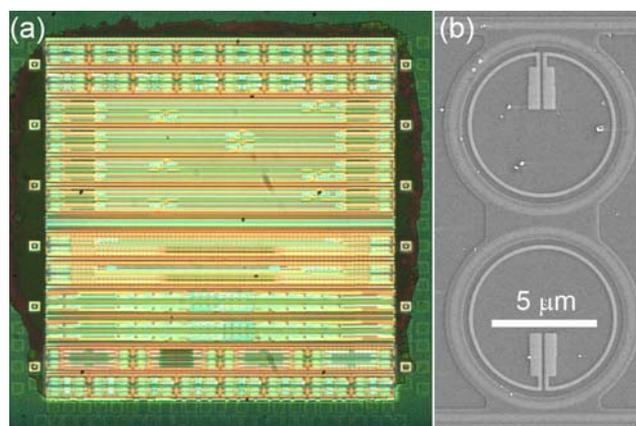
In the past decade, silicon has moved from a work bench for low-index-contrast photonics to a platform for strong-confinement (SC) photonics. SC silicon-core waveguides provide low-loss while enabling micron-scale photonic structures [1] and suitability for next-generation telecom components [2]. As Si performance begins to rival traditional III-V telecom-grade photonics, the possibility of inter- and intrachip photonic interconnects integrated with traditional CMOS electronics opens photonics to the VLSI community [3]. Photonic interconnects have the potential to break increasingly severe energy-efficiency and bandwidth bottlenecks of electrical interconnect in scaled CMOS microprocessors. However, most initial efforts in SC silicon photonics have relied upon specialized processes with limited high-volume CMOS integrability, such as silicon-on-insulator with buried oxide several-microns thick [1-3]. Photonic components required for integration include SC waveguides, resonant add-drop filters for wavelength-division multiplexing (WDM), energy-efficient modulators and integrated photodiodes. In this work, we present a general strategy for photonic integration into bulk CMOS and the first photonic test chip using this approach. The chip, shown in Figure 1(a), was produced in a commercial 65nm process.

## 2. Waveguide integration in a bulk CMOS process

Traditional silicon-on-insulator (SOI) waveguides that use the silicon layer as the waveguide core require a thick buried-oxide layer (2 to 3  $\mu\text{m}$ ) to enable low loss due to optical leakage to the substrate. This increased oxide thickness degrades the thermal-sink properties of the substrate preventing the dense electronic integration required for microprocessors. The photonic chip presented here was produced within a commercial bulk-CMOS process flow, adding zero in-house production changes, ensuring optimal performance of integrated electronic circuits and minimizing production cost.

In bulk CMOS processes, unlike SOI CMOS, there is no single-crystal silicon layer that could be patterned for photonics. Multiple higher-index nitride layers that could potentially be used as waveguide cores are present in the

backend of the CMOS processes, but none are patternable. There is, however, a patternable polysilicon layer in the process front end that is used to form the transistor gates over a thin oxide as well as local interconnects and resistors over a thicker oxide referred to as shallow-trench isolation (STI). Traditionally, the end of line polysilicon is heavily doped and silicided to reduce electrical resistance, resulting in a material with high optical loss. The front-end poly-Si layer must first be deposited undoped since opposite polarity implant steps are used to form the n-channel and p-channel transistor gates. Additionally, the need to create accurate resistors in a mixed-signal process requires a way to block the standard silicidation step of the polysilicon. These two facts allow for the processing masks to be designed to create an undoped, unsilicided polysilicon layer for SC waveguide fabrication. The chief remaining problem is that the sub-400 nm-thick STI, is not sufficiently thick to prevent the optical mode from "leaking" into the Si substrate. Although this problem could be solved by modifying the standard process to include thicker STI regions, we propose to introduce a sufficiently thick air-pocket locally under waveguide cores by a self-aligned, scalable post-processing step. An implementation of such a step is proposed and demonstrated in [4].



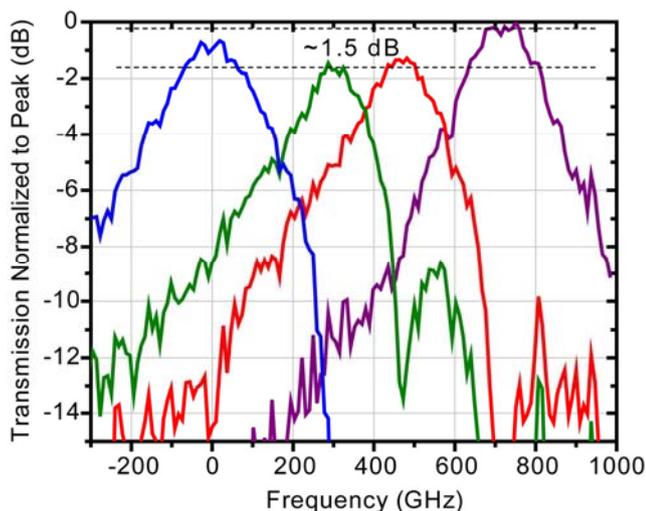
**Figure 1 : (a) Bulk 65 nm photonic test chip die, photographed from the substrate side after removal of the silicon substrate. (b) Scanning-electron micrograph of second-order ring-resonator filter, exposed by etching STI layer following Si-substrate removal.**

To integrate the large, arbitrarily-curved structures required for photonics within the Manhattan-geometry standard IC design environment, a suite of geometric sub-routines and parameterized photonic device cells was developed within Cadence's Virtuoso suite. The photonic-structure layout is produced as a combination of rectangular strips on the

CMOS mask address grid given a small set of device design parameters. Additionally, the standard metal fill, used in CMOS processes to ensure backend-process uniformity, had to be excluded and replaced with custom fill blocks to ensure that local-density requirements are met around the photonic structures, without placing metal in close proximity, which would cause excess waveguide loss.

### 3. 65 nm-node bulk-CMOS photonic test chip

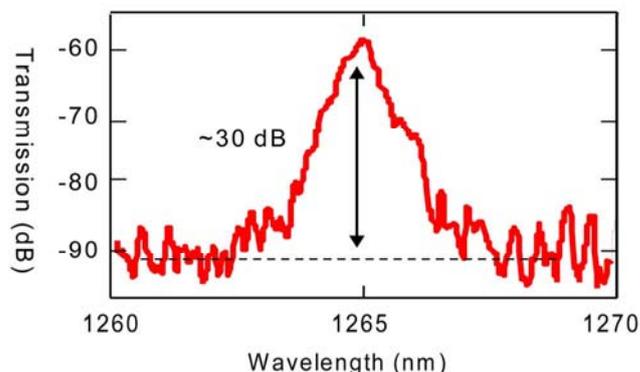
Using this platform, we designed the first photonic chip in a commercial bulk-CMOS process on a 4 mm<sup>2</sup> die. Primary chip goals were to demonstrate integrability, characterize waveguide loss and evaluate photonic-device performance. In total we incorporated 116 independently-addressable test structures containing over 21 cm of waveguides. Additionally, high-speed modulator drivers with data-input signal-processing electronics were included, designed to demonstrate integration with photonics without electronic device performance degradation. The latter is guaranteed since the only post-processing on the die is localized to within a few microns of the photonic devices.



**Figure 2 : Drop-port transmission functions from a 4-channel filter bank with ~240 GHz channel spacing. The dynamic range is limited by the IR camera used in this measurement.**

The photonic devices on this die included microheater-tuned ring-resonator filters, carrier-injection modulators, Mach-Zehnder interferometers, low-loss Bloch-wave crossings [5] and polysilicon photodiodes. The operating wavelength was around 1220 nm in anticipation of the future inclusion of silicon-germanium photodiodes, based on the existing epitaxial steps present for p-channel strain engineering. Vertical-grating-couplers were used for dense integration and the potential of future wafer level testability, but all critical structures were also accessible via cleaved-facet coupling. Vertical-grating-coupler insertion loss of 8.2 dB was achieved, closely matching the 7.1 dB design simulations. Initial photonic-device tests on the die were performed after complete substrate removal and demonstrate basic functionality. First-order ring-resonator filter banks formed by stepping the ring radius by 5 nm

produced correctly ordered filters with low variability, as shown in Figure 2. Second-order ring-resonator filters demonstrated ~30 dB drop-port extinction ratios, as shown in Figure 3. An SEM of this filter demonstrating no apparent lithographic distortion is shown in Figure 1(b).



**Figure 3 : Drop-port transmission for a second-order ring resonator filter. Drop-port 3 dB bandwidth is approximately 130 GHz.**

### 4. Conclusion

Add-drop filter banks for wavelength channel routing have been demonstrated in a CMOS platform. The platform satisfies the needs of many applications of SC silicon photonics while allowing dense electronic integration. Since the photonic devices were produced with zero in-foundry modifications, optimum electronic device functionality is guaranteed.

### 5. Acknowledgment

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