

# A Fractionally Spaced Linear Receive Equalizer with Voltage-to-Time Conversion

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## Abstract

Based on voltage-to-time conversion technique, a pseudo-differential two-way-interleaved adaptive linear receive equalizer with two 2x-oversampled feed-forward taps has been designed in a 90 nm CMOS process. It integrates equalization and phase interpolation functions into one unit to simultaneously address inter-symbol-interference (ISI) cancellation and phase synchronization in a link receiver. It operates at 4 Gbps with 8 mW power consumption, and linearity of 4.3 effective bits at 1.2 V supply.

Keywords: fractionally spaced receiver equalizer

## Introduction

Intersymbol-interference (ISI) is becoming an increasingly severe issue as target data rates increase in link applications, challenging both the equalization and synchronization sub-systems. Traditionally, adaptation loops in these two sub-systems derive the error information from different performance metrics (voltage errors at data sampling points and error information at edge crossings). This discrepancy results in sub-optimal link performance due to the interaction of the two loops, especially in situations where received signals are significantly asymmetrical and distorted by ISI [1,2] (e.g. loop-unrolled decision-feedback equalizers).

Fractionally spaced equalizers enable controlled ISI reduction at arbitrary sampling phase with a single adaptation loop [3]. In this paper we describe an implementation of a two 2x oversampled feed-forward taps receiver equalizer structure. Apart from oversampling speed challenges, implementation of linear receiver equalizers has been a difficult problem due to process mismatch and speed-power-nonlinearity trade-offs in current-mode implementations in scaled, low-supply voltage CMOS processes [4].

## Architecture

To overcome these issues with good energy-efficiency, and achieve 4~5 bit linearity required by the adaptive algorithm the FSE design is based on voltage-to-time and time-to-voltage conversion techniques [5]. Due to the process speed limitation, half-rate time interleaving technique is also applied, Fig. 1. Four sampling phases ( $\Phi_1$ - $\Phi_4$ ) with 25% duty cycle are generated locally from  $\Phi$  and  $\Phi_{\bar{}}$  and another pair of quadrature clocks. A voltage-to-time (V2T) block converts the sampled signal into a delayed digital signal, transferring the sampled information into time-domain. All four V2T converters are followed by a time-to-voltage (T2V) stage to realize summing, subtraction and multiplication.

Equalizer tap weights are implemented as two programmable reference currents  $I_1$ ,  $I_2$  biasing T2V blocks. Two slicers with tunable thresholds are added to sense the signs of the input signal and output error of the FSE, respectively, and enable tap weight adaptation with external adaptive engine.

## Implementation

### A. V2T Converter

The V2T converter is shown in Fig. 2. When clock  $\Phi_{\bar{}}$  is low, nodes  $V_{S+}/V_{S-}$  are pre-charged to VDD. Simultaneously, the sampling capacitors  $C_{S+}/C_{S-}$  track the input signals. The following edge of  $\Phi_{\bar{}}$  pulls the sampled voltages on nodes  $V_{X+}/V_{X-}$  down by the same amount so that they are lower than the threshold voltage at the initial state. Afterwards, two identical currents  $I_{\text{charge}+/-}$  charge  $V_{X+}/V_{X-}$  respectively. The nodes  $V_{X+}/V_{X-}$  will reach the threshold of  $N+/-$  at different times and trigger two pairs of edges ( $E_{1r+/-}$  and  $E_{1r+/-}$ ). To shorten the decision time,  $P+/P-$  provide positive feedback, improving the design speed by roughly 30%, for target time dynamic range. The timing  $\Delta t$  between  $E_{1r+}/E_{1r+}$  and  $E_{1r-}/E_{1r-}$  is proportional to the differential input  $V_{\text{in}1}$ .

### B. T2V Converter

The T2V converter operation is shown in Fig. 3, with waveforms for  $I_2=0$  for simplicity. When  $\Phi_{\bar{}}$  is low, output nodes  $V_{O+}/V_{O-}$  are pre-charged to VDD. After the rising edge of  $\Phi_{\bar{}}$ , nodes  $V_{O+}/V_{O-}$  are discharged with current  $I_1$  since  $E_{1f+}/E_{1f-}$  are high and  $E_{1r+}/E_{1r-}$  are low. After the arrival of  $E_{1f+}/E_{1r+}$  edges, the discharge current by  $M_{1+}$  switches from  $V_{O+}$  to  $V_{O-}$ . Therefore, the discharge current of  $V_{O+}$  becomes zero and that of  $V_{O-}$  is doubled. Thus, the difference between  $V_{O+}$  and  $V_{O-}$  increases from zero till the arrival of  $E_{1f-}/E_{1r-}$  edges. Afterwards, the current by  $M_{1-}$  is rerouted to  $V_{O+}$  and the discharge currents for both are  $I_1$  again, and  $V_{O+/-}$  decrease with the same slope until the falling edge of  $\Phi_{\bar{}}$ . The voltage output  $\Delta V_O$  is proportional to  $V_{\text{diff.in}1} \times I_1$  and  $V_{\text{diff.in}2} \times I_2$ , implementing the multiplication and summing operations. Changing the sign multiplexer control will realize a subtraction. T2V integrator has significantly improved linearity over the traditional GmC stage since its inputs are always full swing signals.

## Measurements

The design is fabricated in a 90 nm CMOS process. The chip layout is shown in Fig. 4, with additional support blocks like scan chain and high-speed data snapshots to enable link tuning and in-situ performance characterization. The FSE receiver area is 65  $\mu\text{m}$  x 130  $\mu\text{m}$ .

At 4 Gbps rate, tuning the tap weights guarantees a flat open eye within +/-5% for any delay between data and clock, compared to the eyes visible by symbol-spaced slicers, Fig. 5b. Due to larger than predicted parasitic capacitance at the  $V_X$  node in the V2T converter, the design exhibits about 2x attenuation at  $V_O$  with respect to the input signal, Fig. 5a, but achieves target linearity of 4.3 effective bits with monotonic gain in tap weights, Fig. 6.

## Conclusion

Leveraging the speed of advanced digital processes, a voltage-to-time conversion techniques provide an effective way to overcome the linearity issues in high-speed link receive filters and enable the implementation of fractionally-spaced filters that simultaneously address the phase synchronization and equalization tasks with good energy-efficiency.

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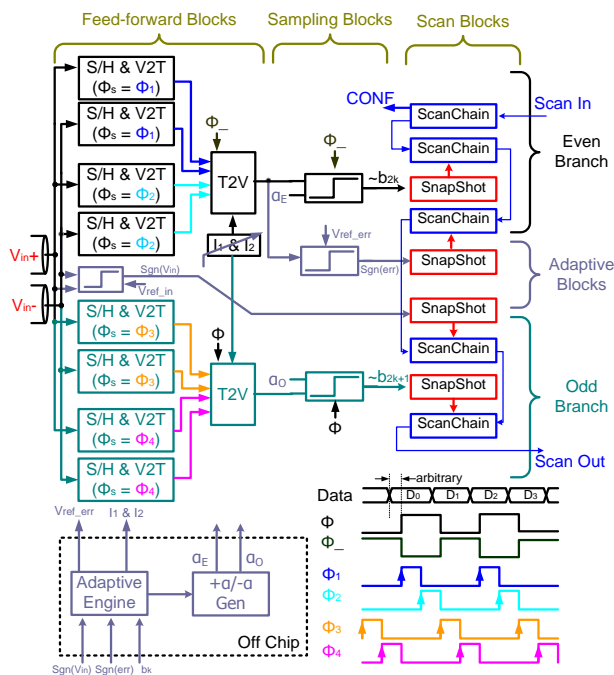


Fig. 1 Block diagram of 2-tap 2xoversampled two-way time interleaved architecture. Scan-chain and snapshot are applied for *in-situ* link characterization.

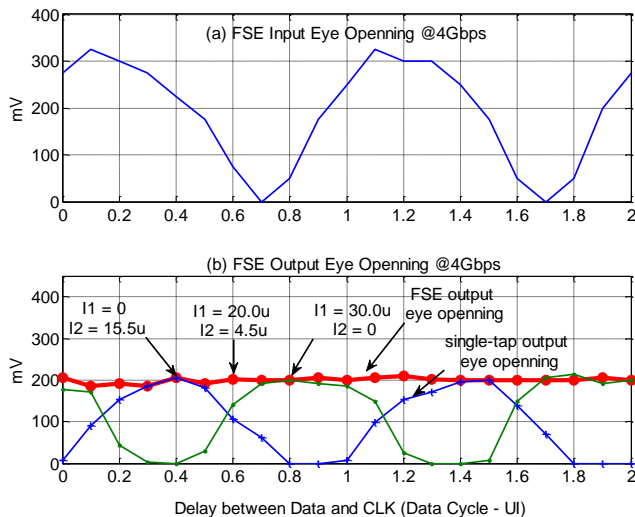


Fig. 5 Input (a), and FSE output (b) eye opening vs. sampling phase.

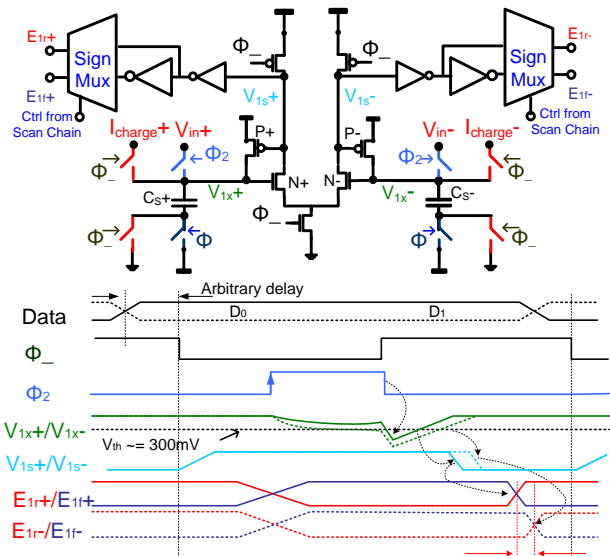


Fig. 2 Schematic and time diagram of V2T converter

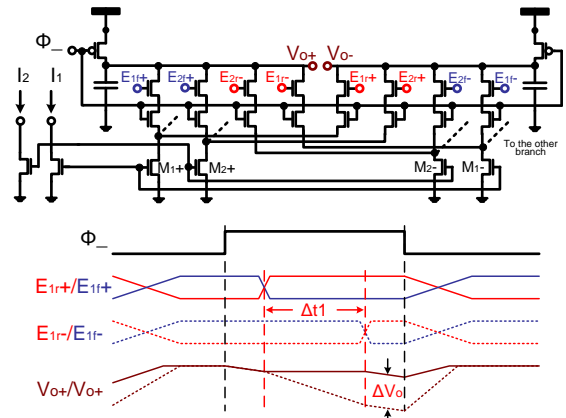


Fig. 3 Schematic and time diagram of T2V converter when  $I_1 > 0$  and  $I_2 = 0$ .  $M_{1+}$ ,  $M_{1-}$ ,  $M_{2+}$  and  $M_{2-}$  are shared by even/odd branches.

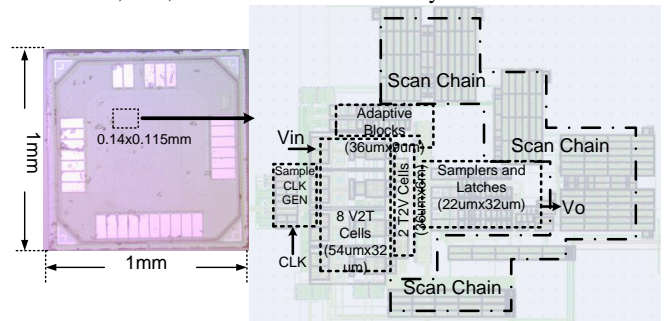


Fig. 4 Die photo and chip floor plan.

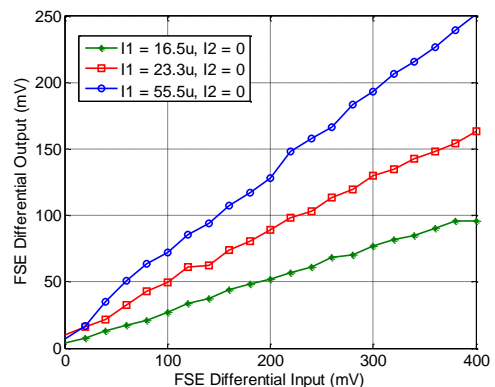


Fig. 6 Linearity of the FSE for different tap weights.