A Fractionally Spaced Linear Receive Equalizer with Voltage-to-time Conversion

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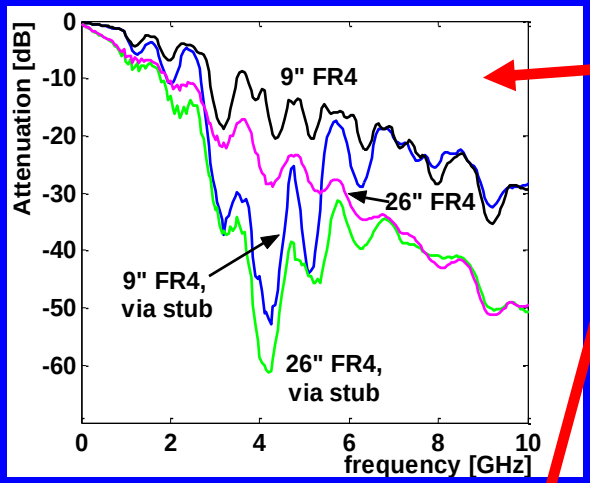
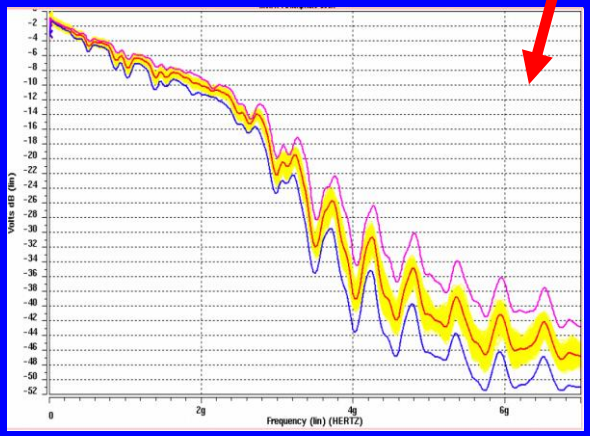
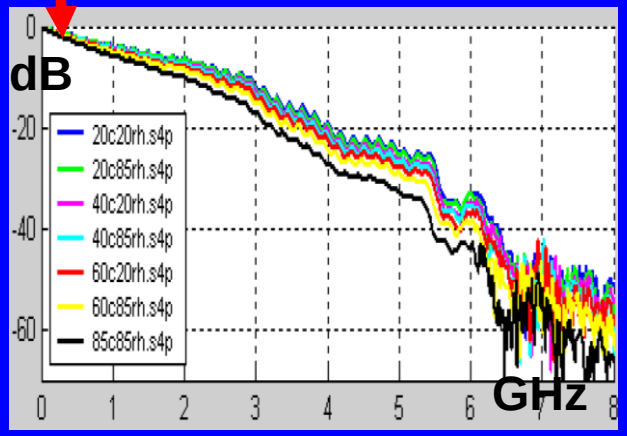
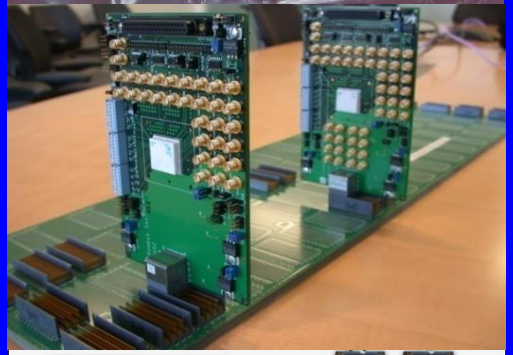
BW limited channels challenge CDR and EQ

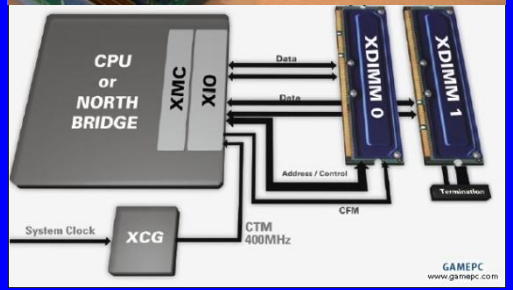


- Trace routing
- Manufacturing
- Temperature & humidity



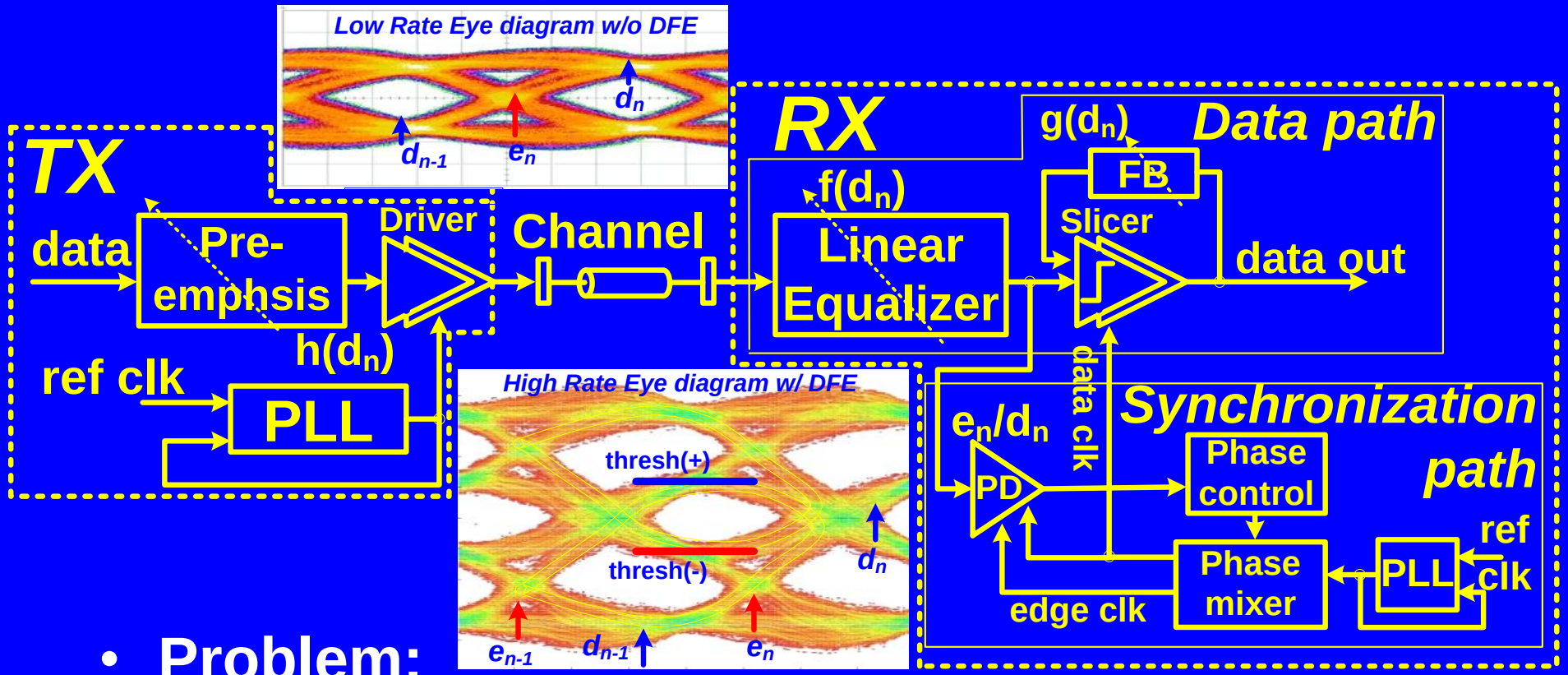






Equalization and synchronization dominate link performance and power efficiency

Interaction between data and synchronization paths in conventional designs

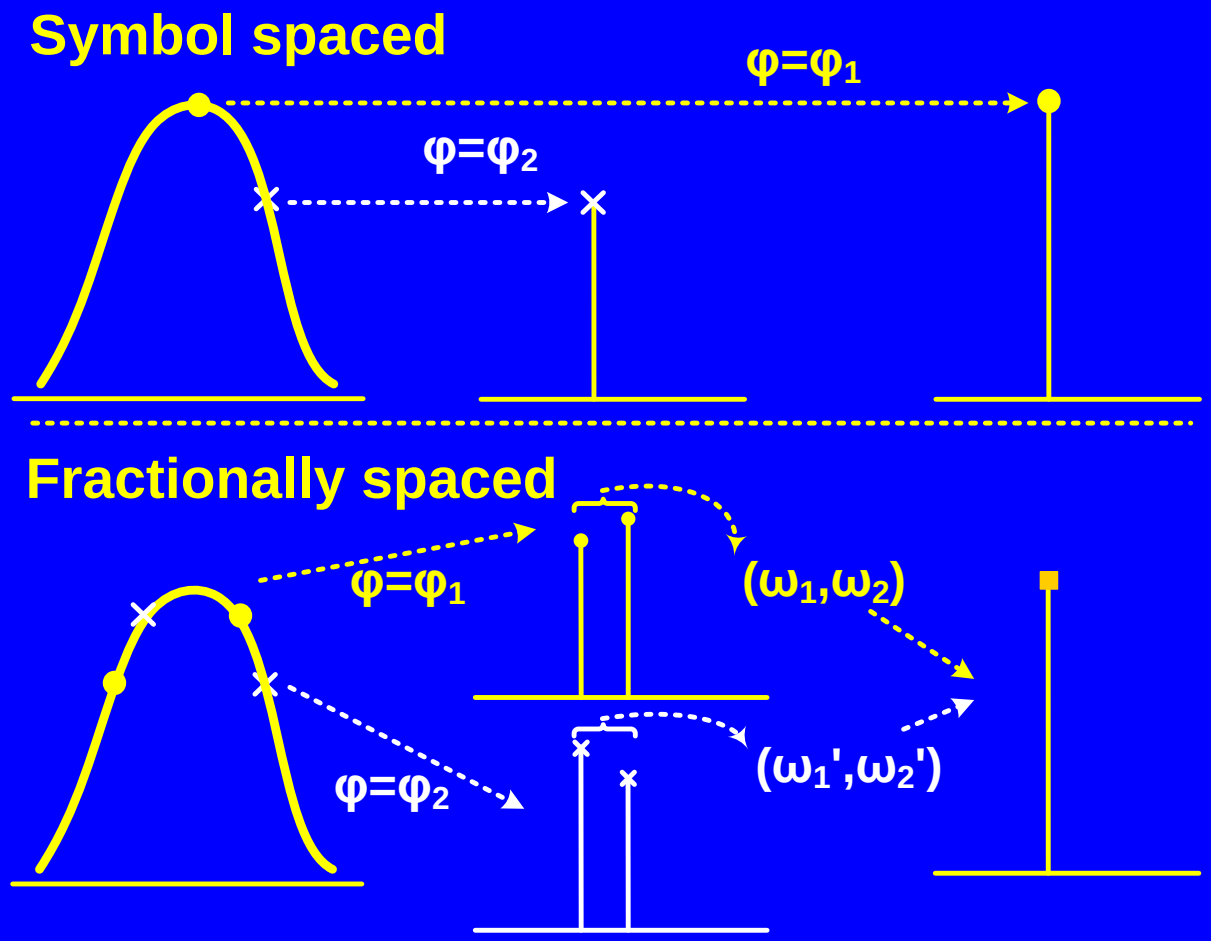


- **Problem:**
  - Equalize on d_n; synchronize on e_n
  - EQ and CDR do NOT work to optimize the same performance metric

Overcoming the limitations

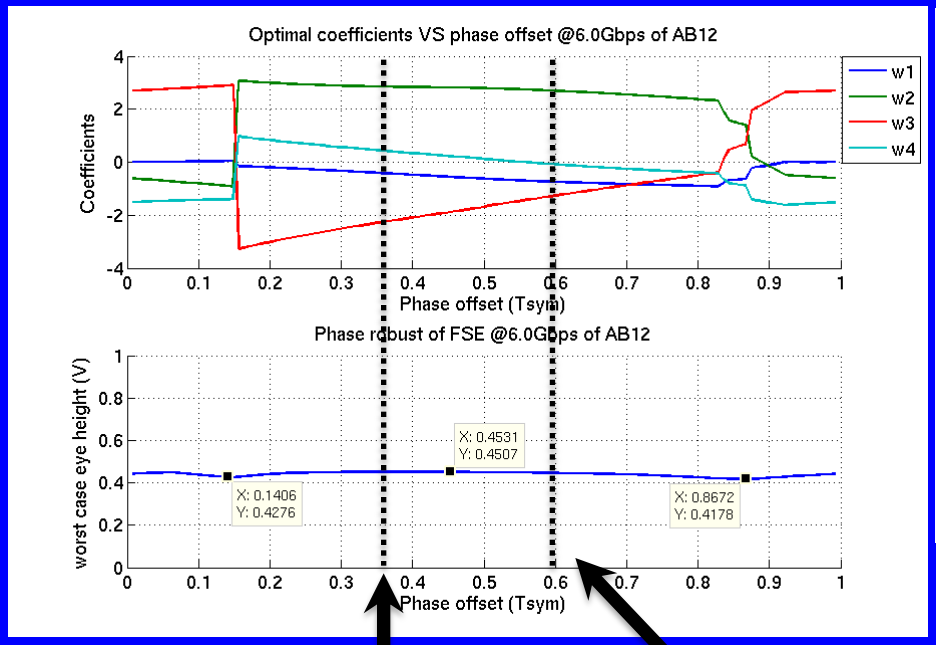
- Performance improvement by joint equalization and phase recovery
- Fractionally spaced equalization (FSE) can do both for mesochronous system
  - Architecture
  - Implementation
  - Measurements

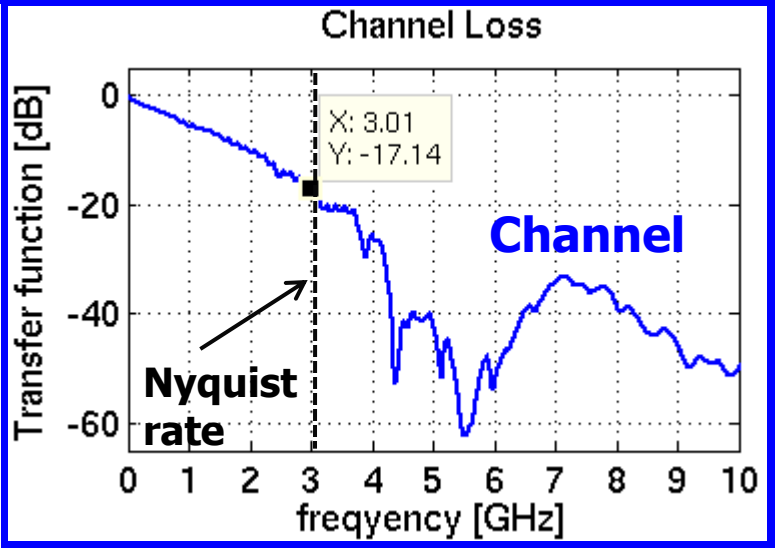
FSE concept



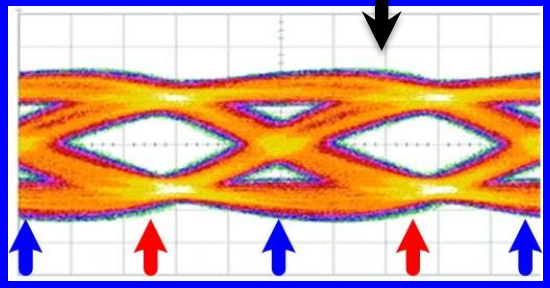
- Phase critical for symbol spaced RX
- FSE compensates phase offset by interpolating samples

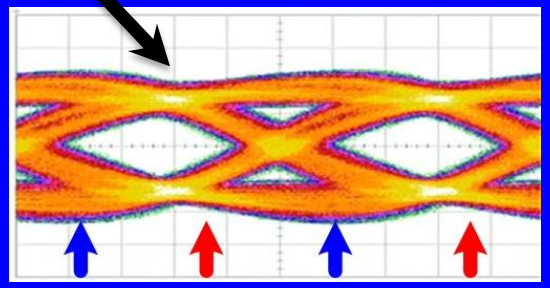
FSE robustness to phase offset





17 dB attenuation at Nyquist rate





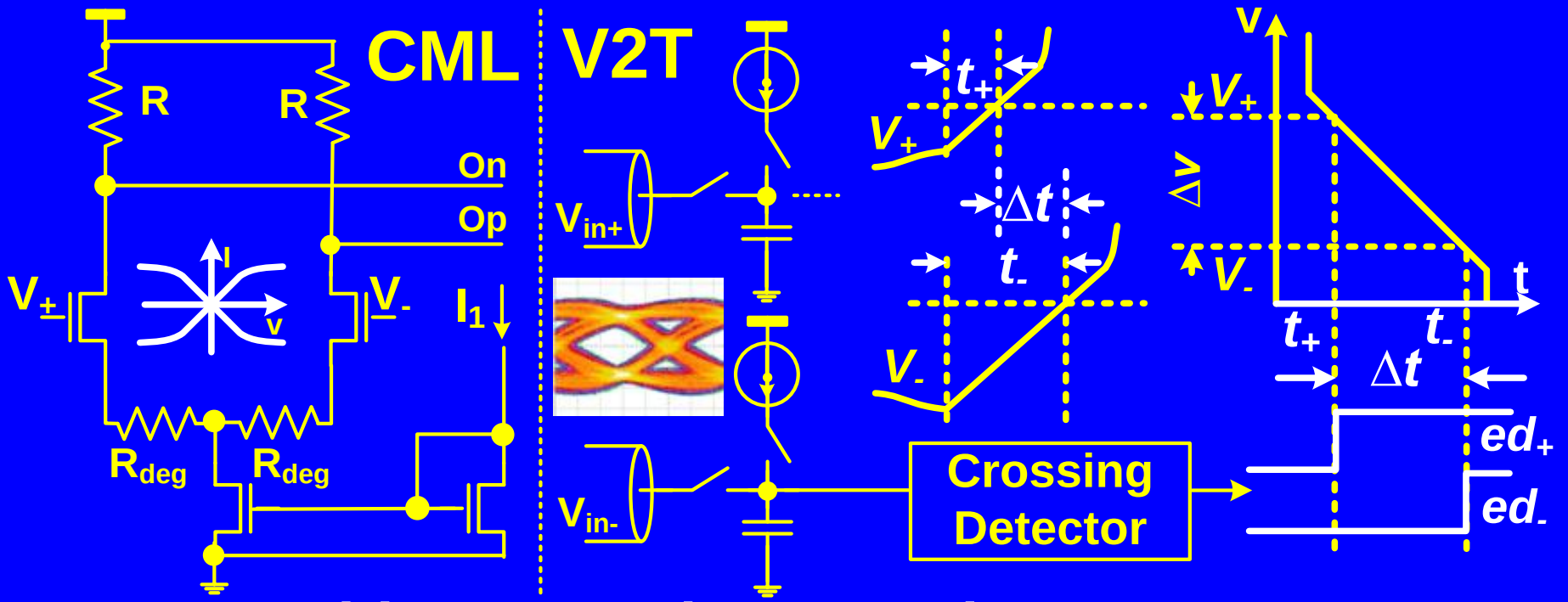
- **Example**
  - **– 4-tap 2X oversampled FSE @ 6Gbps rate**

FSE implementation challenges and options

- **Challenges**
  - **4~5 bit linearity for large DR**
  - **Two samples per symbol period: efficiency**
- **Options**
  - **CML technique**
  - **Voltage-time conversion technique***
    - ***V2T: voltage-to-time converter***
    - ***T2V: time-to-voltage converter***

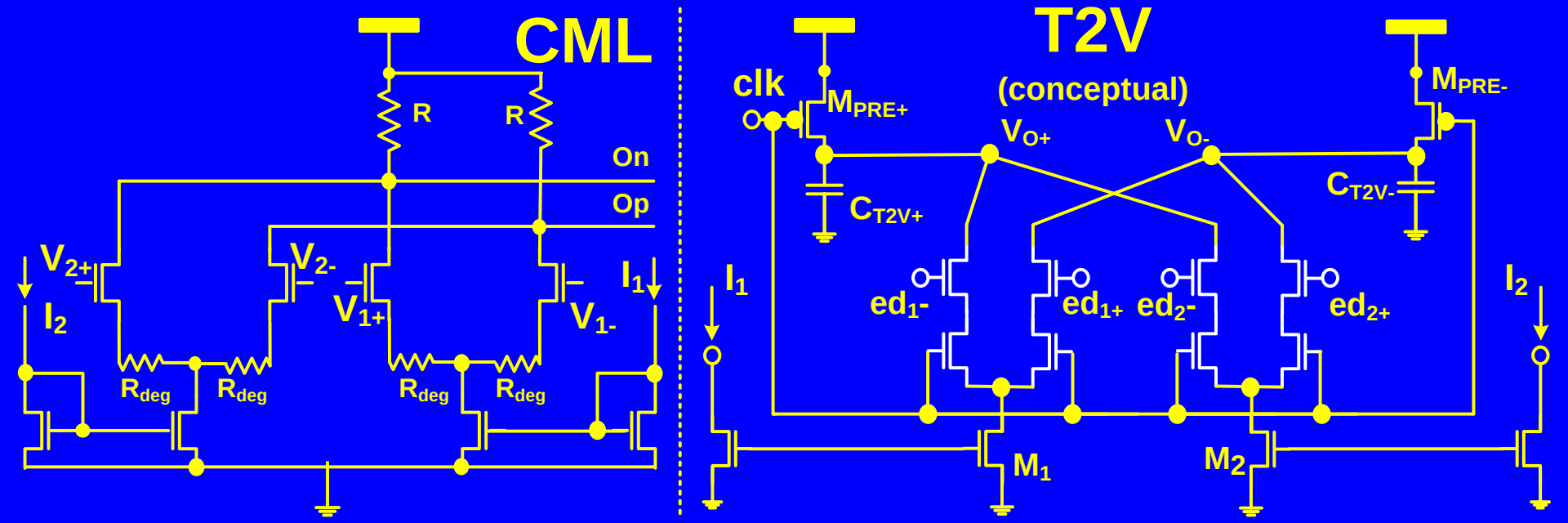
*: ***L. Brooks, H.-S. Lee, "A zero-crossing-based 8b 200 MS/s pipelined ADC," JSSCC, Dec. 2007***

Voltage conversion technique comparisons (1)



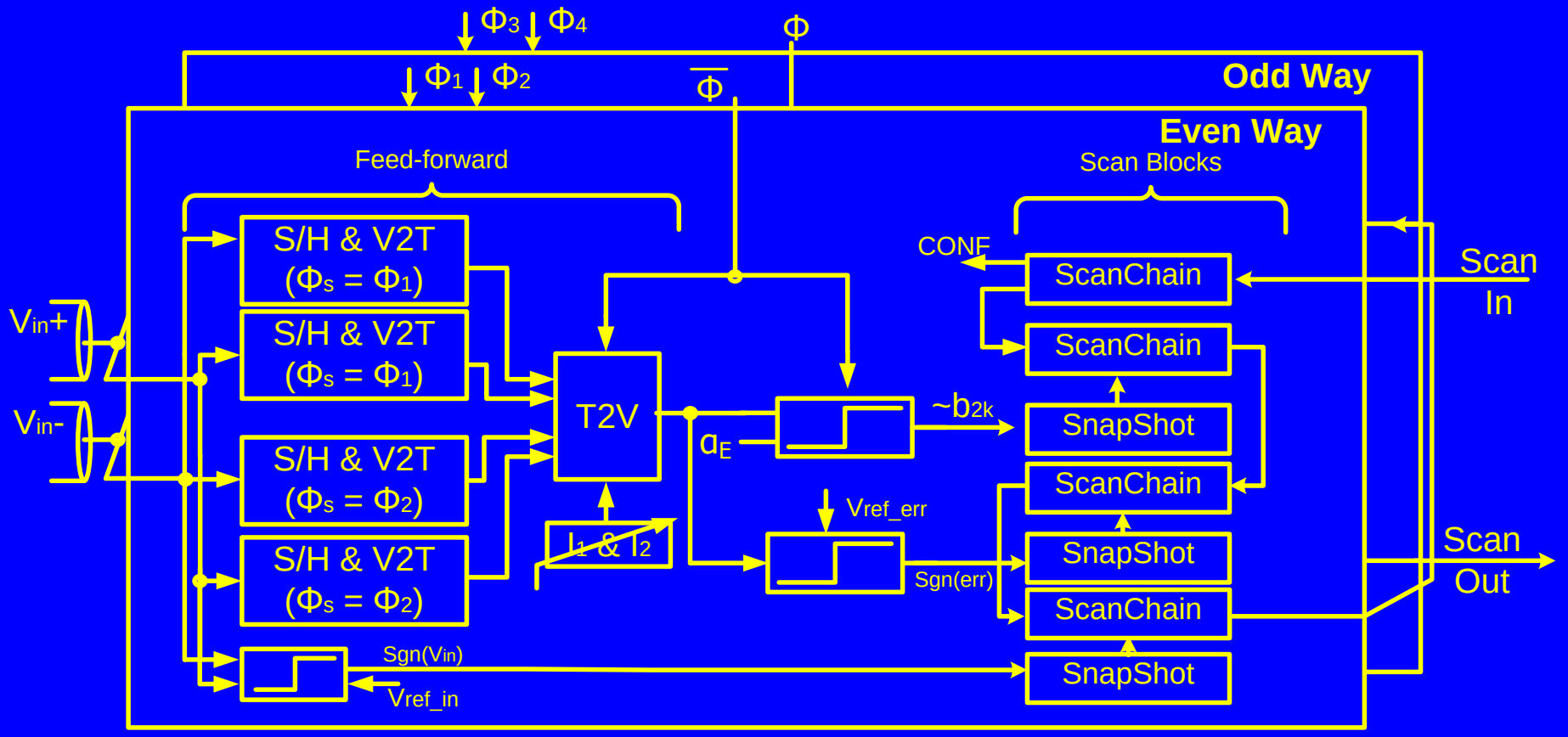
- CML with source degeneration
  - Good linearity with small input signals
  - Bad linearity given large input dynamic range
- V2T
  - Convert by current integration
  - Current sources determine the linearity

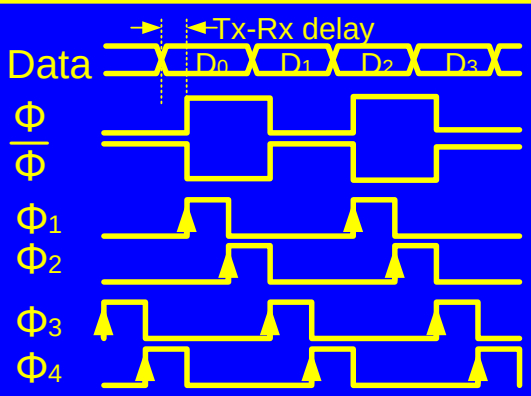
Voltage conversion technique comparisons (2)



- **CML with source degeneration**
  - **Bad linearity when $I_1 << I_2$ & large input DR**
- **V2T**
  - **Timing inputs $ed_{x\pm}$ are digital**
    - **More headroom at V_{O+}/V_{O-}**
  - **>25% power saving than CML**
    - **1.0V VDD & >5bit linearity**

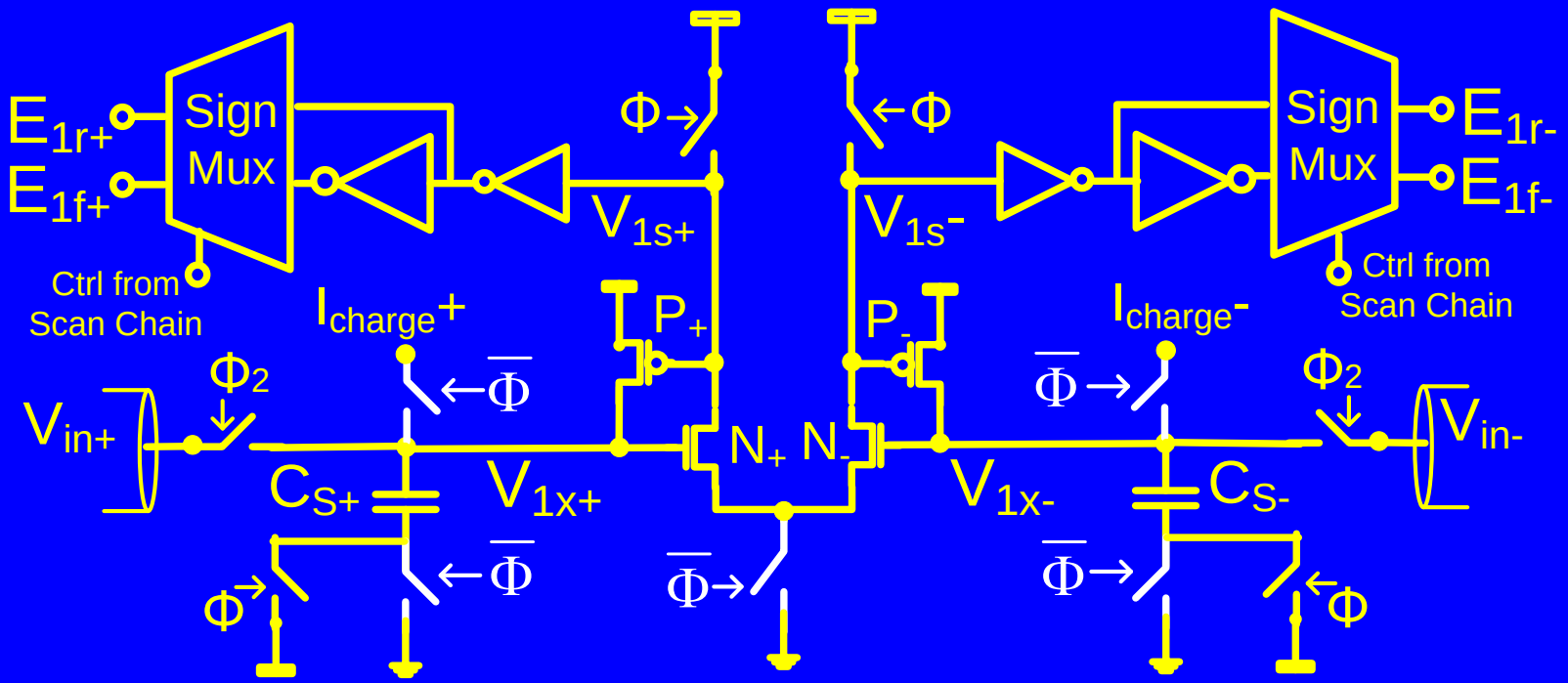
Proposed fractionally spaced equalizer structure

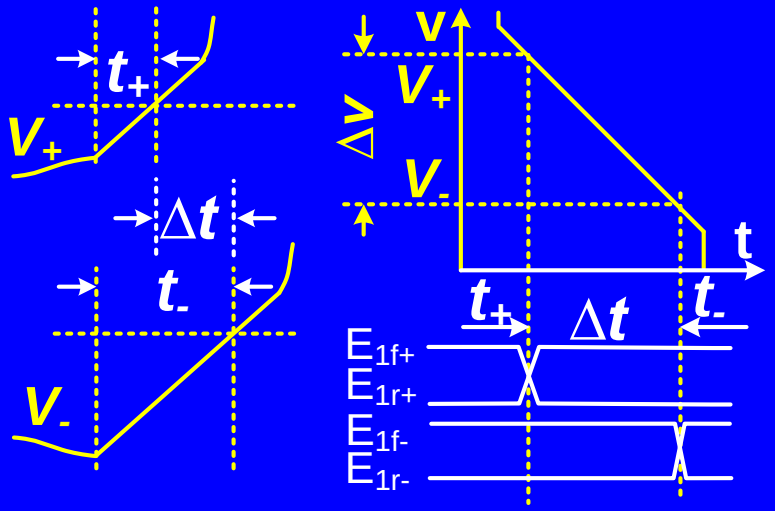




- 2 way interleaving
- 2X oversampling
- 2 feed forward taps

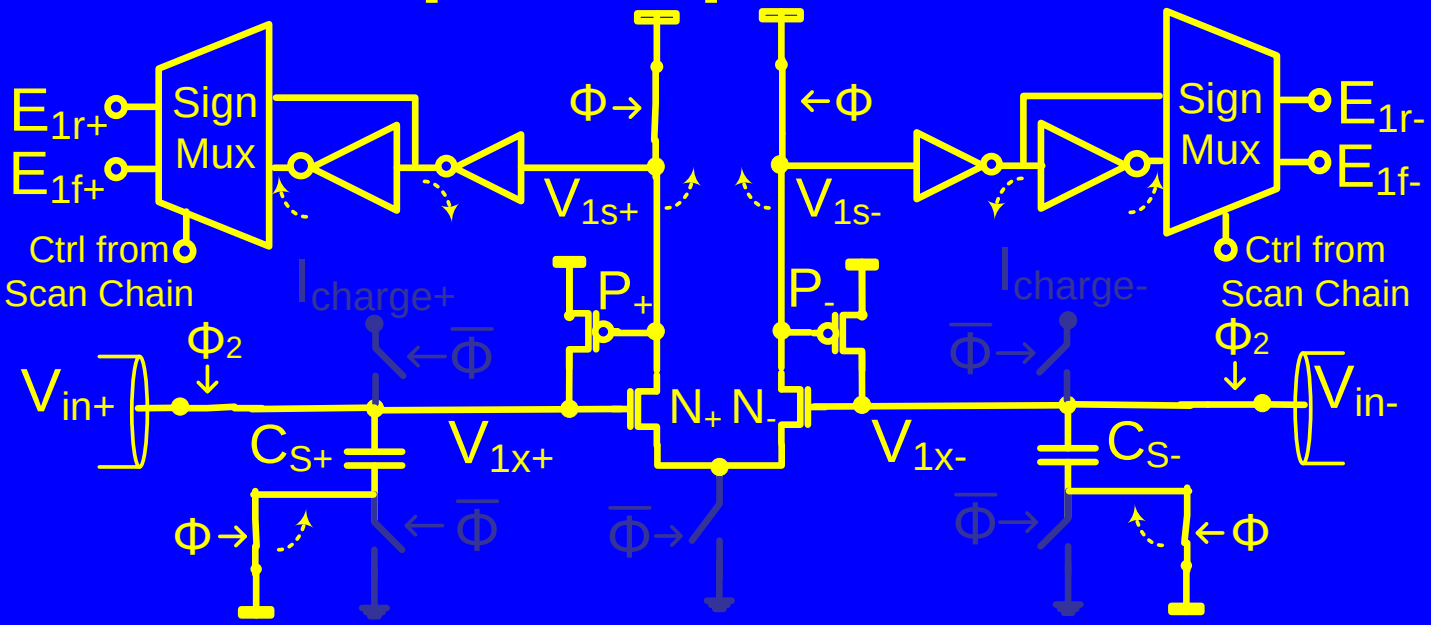
Voltage-to-time converter

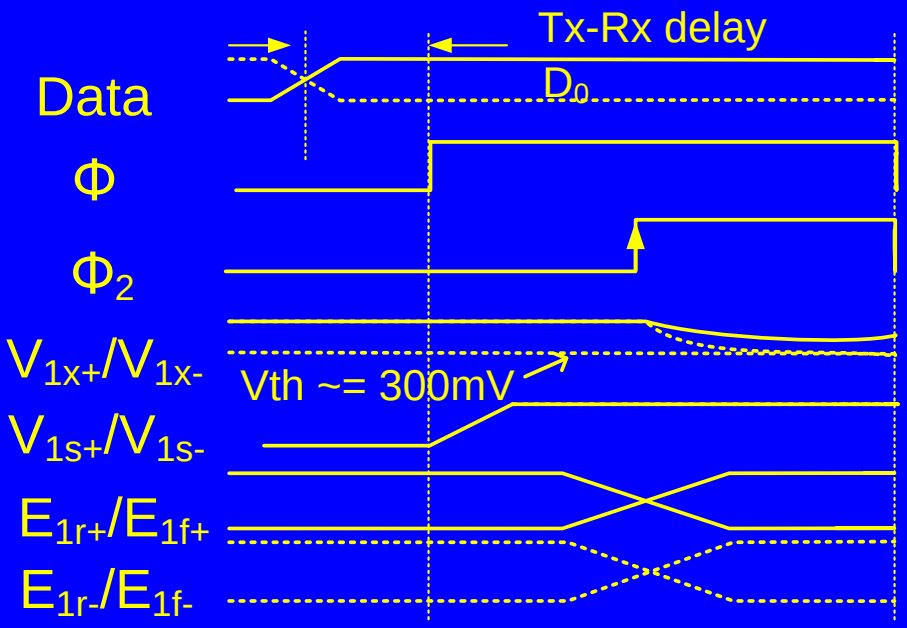




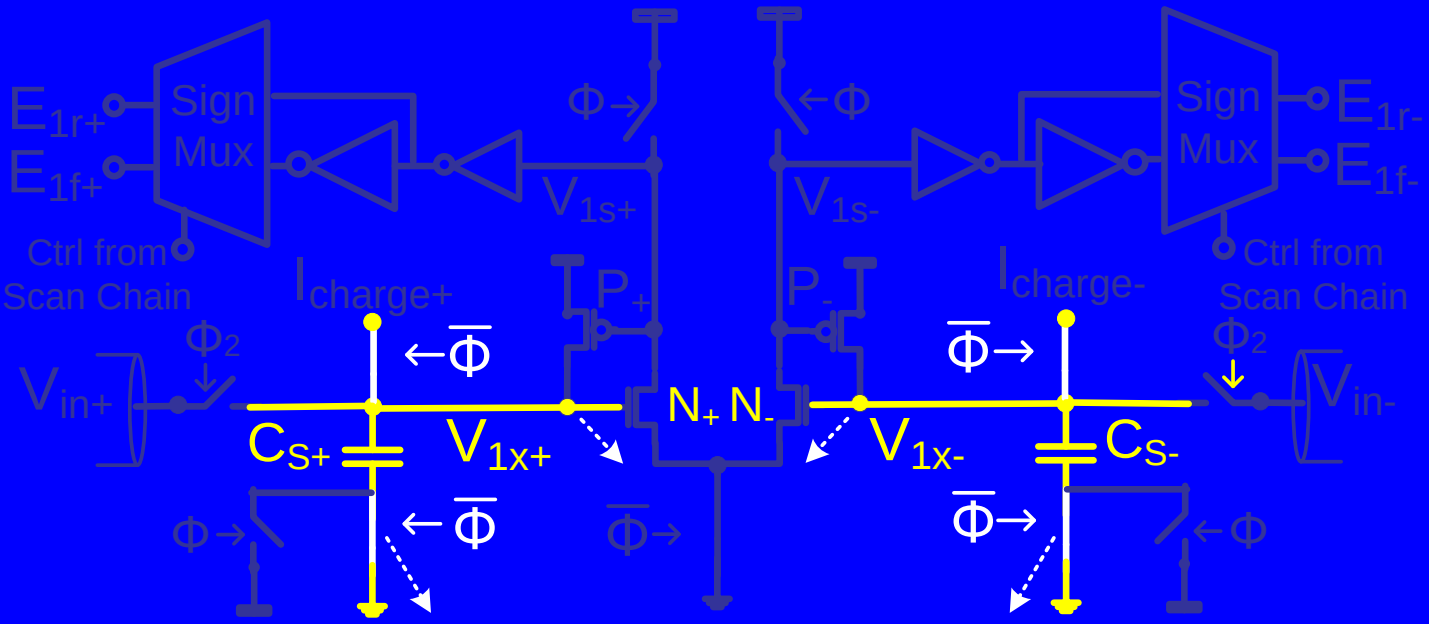
$$\Delta t = a\Delta V_{in}$$

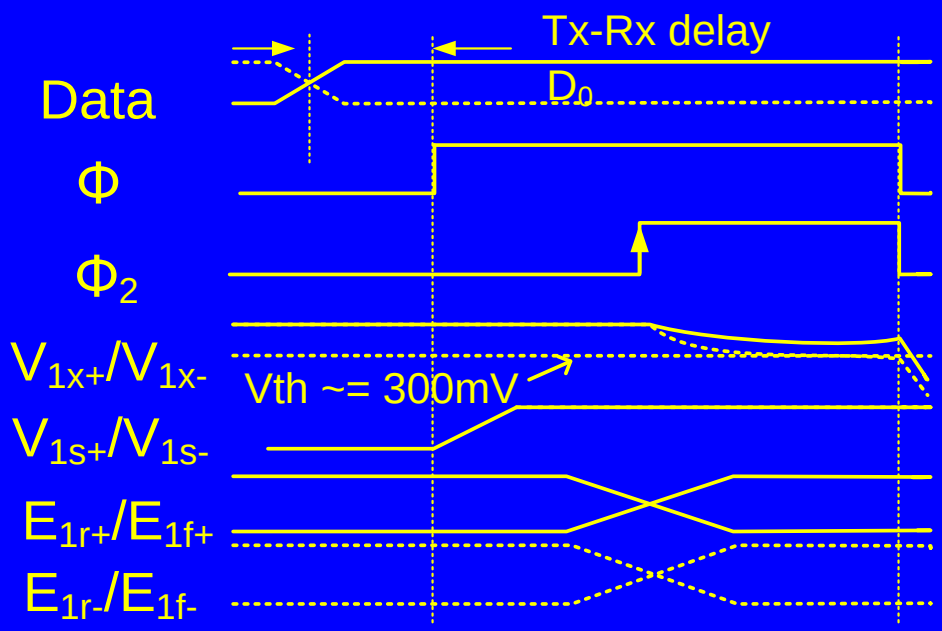
V2T — track & preset phase



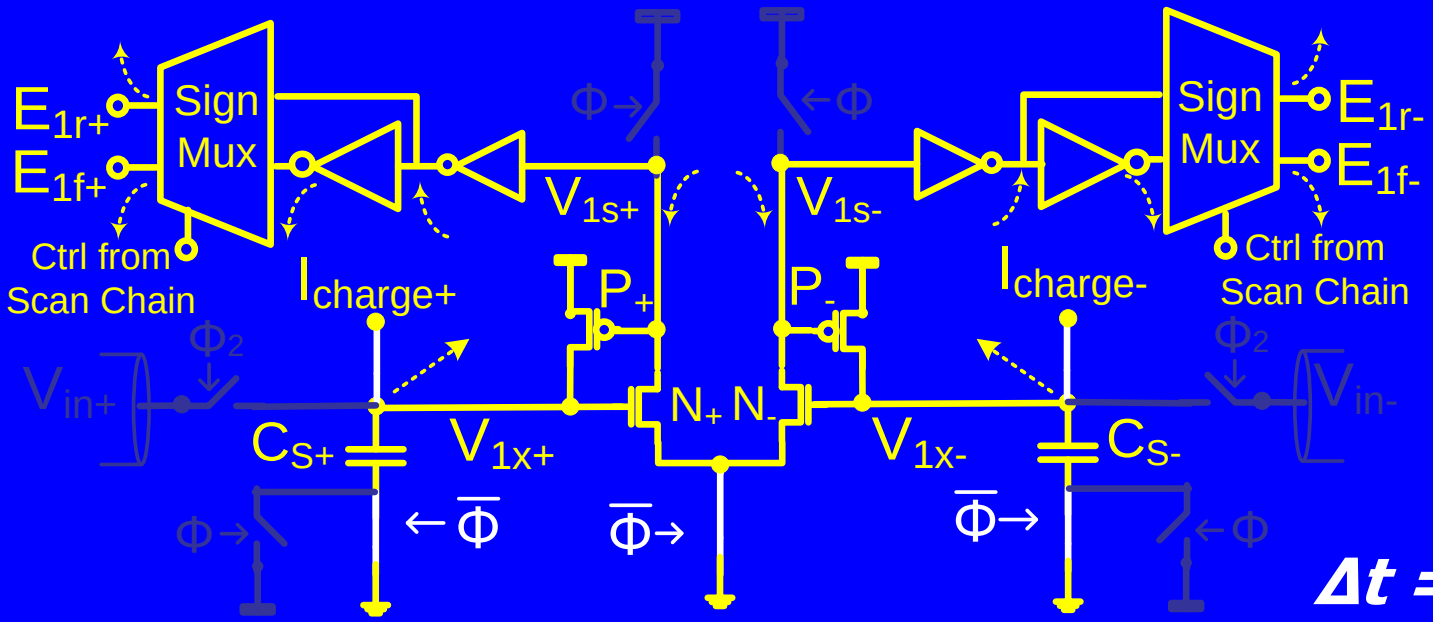


V2T — evaluation phase: sample & level shift

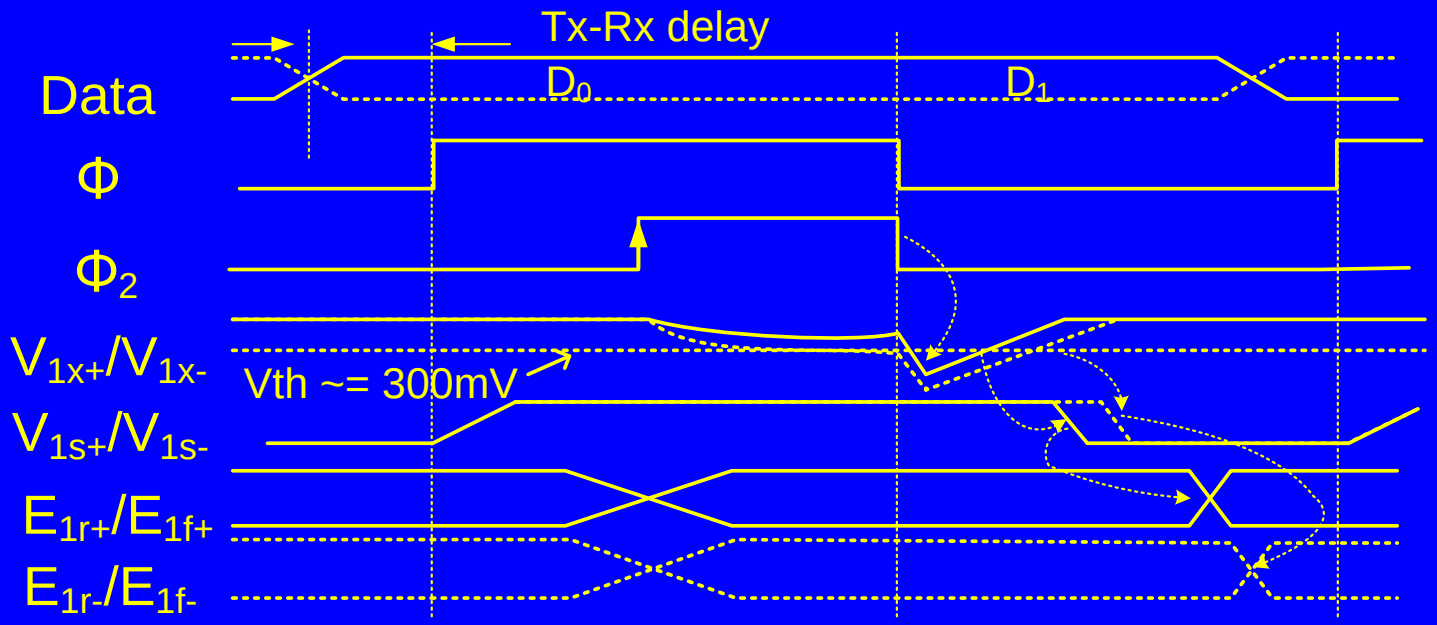




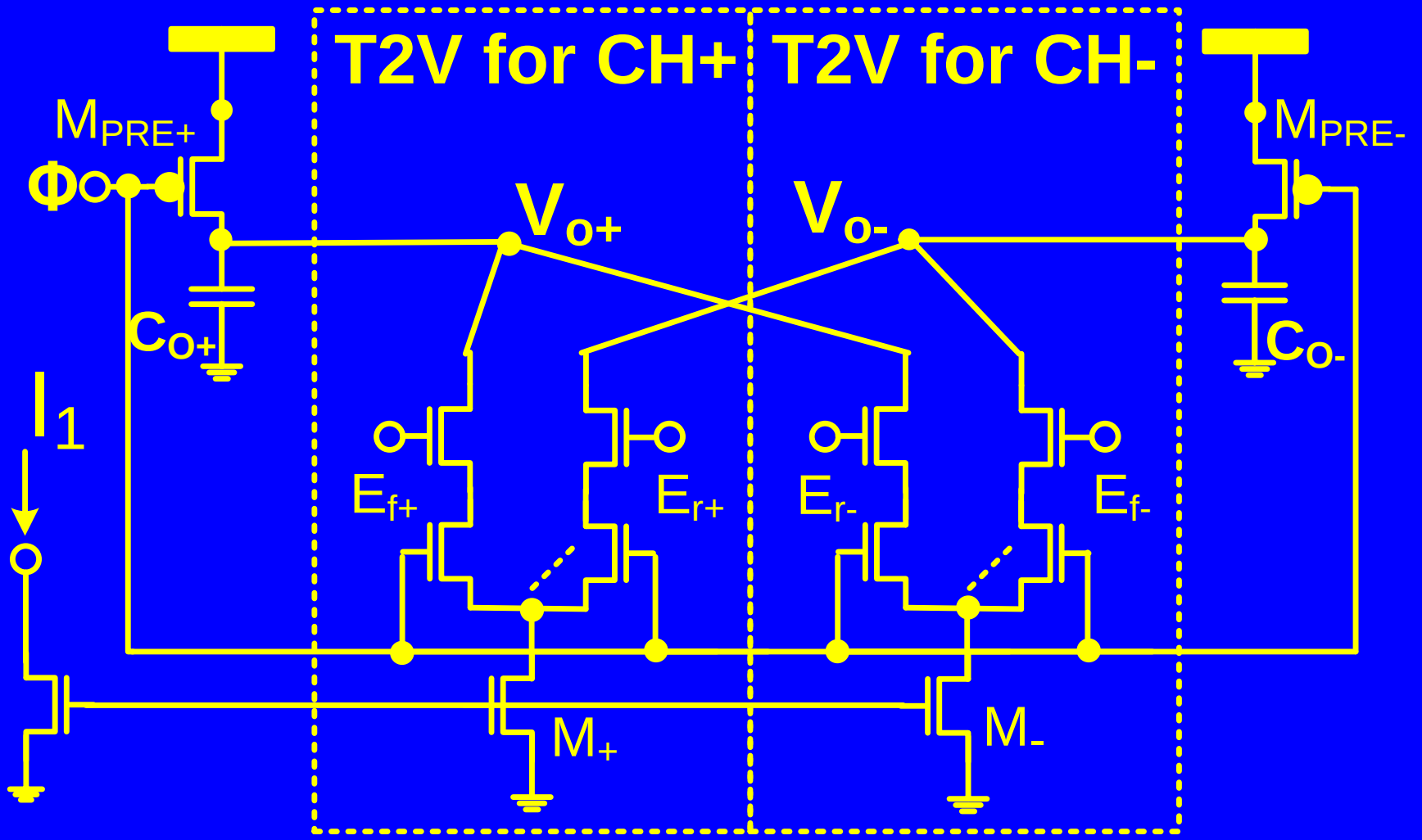
V2T — evaluation phase: ramp-up



$\Delta t = a\Delta V_{in}$

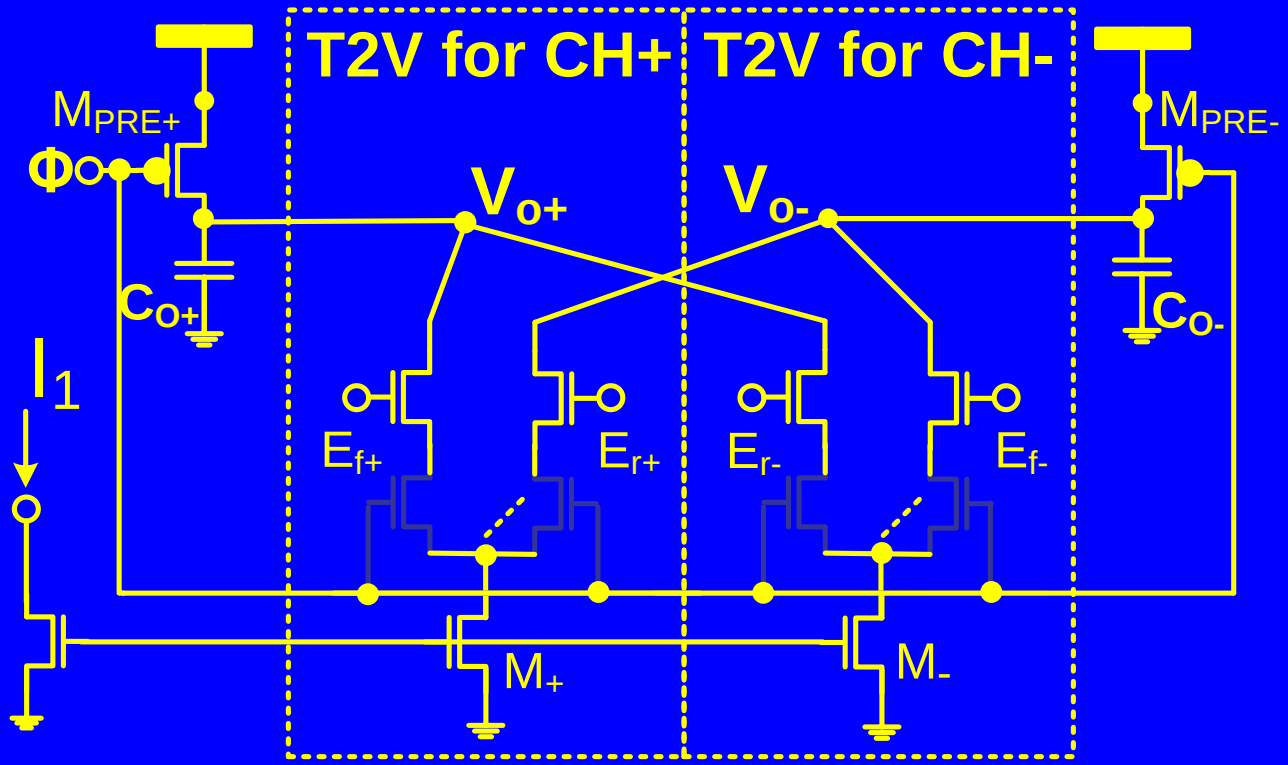


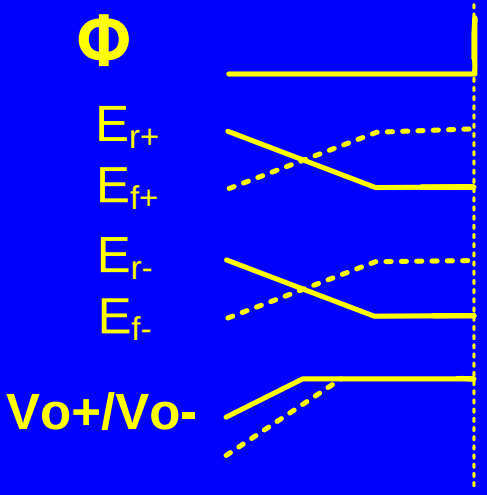
T2V for one tap



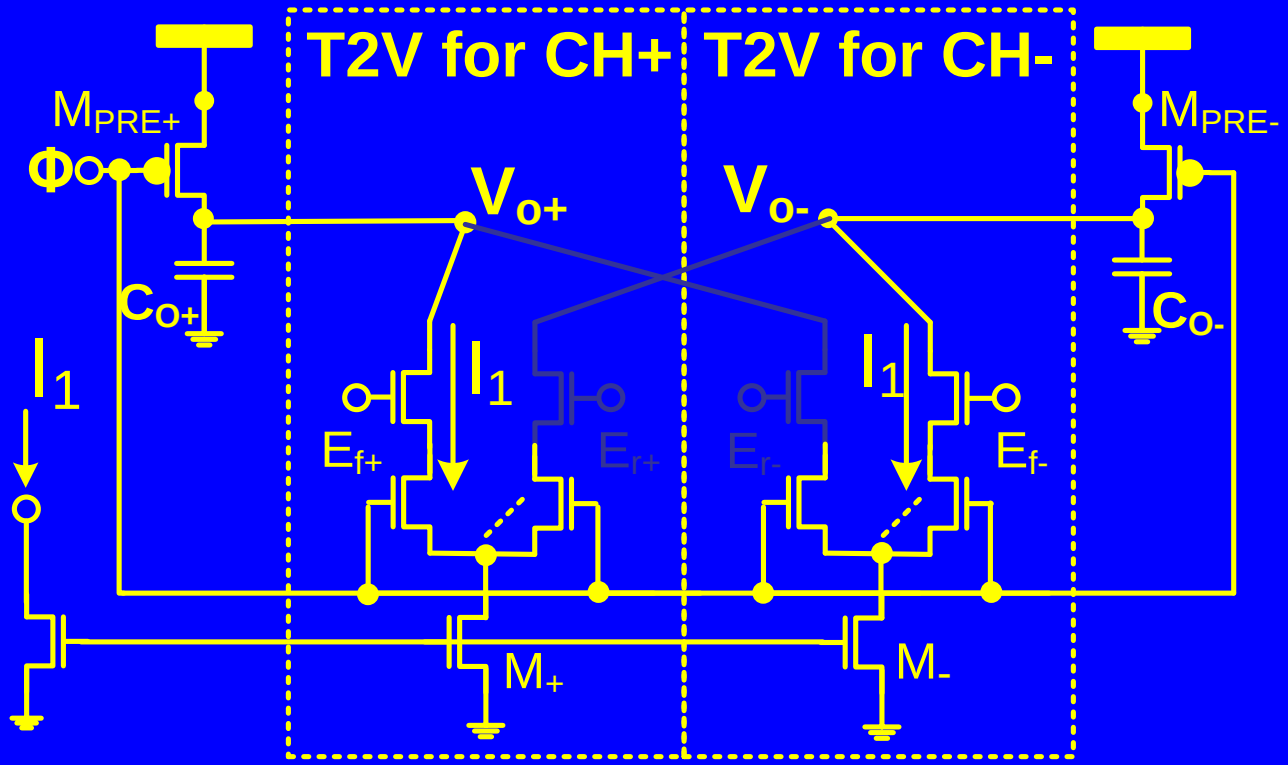
$$\Delta V_O = \mu \Delta t \, I_1 = \mu a \Delta V_{in} \, I_1$$

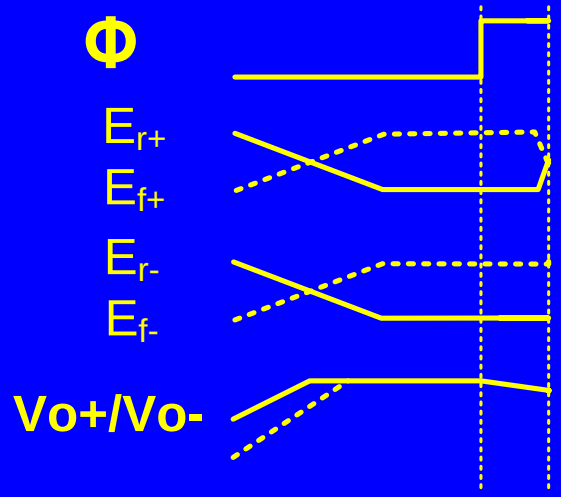
T2V for one tap — preset



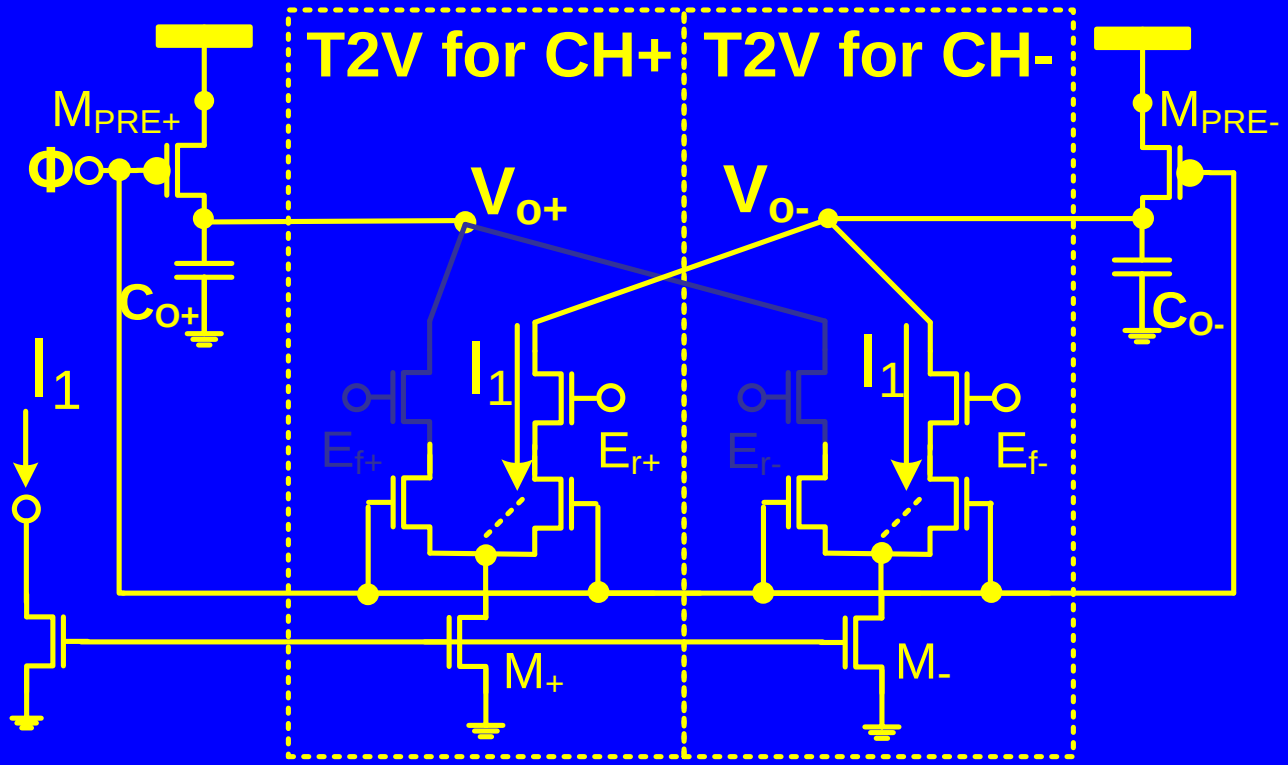


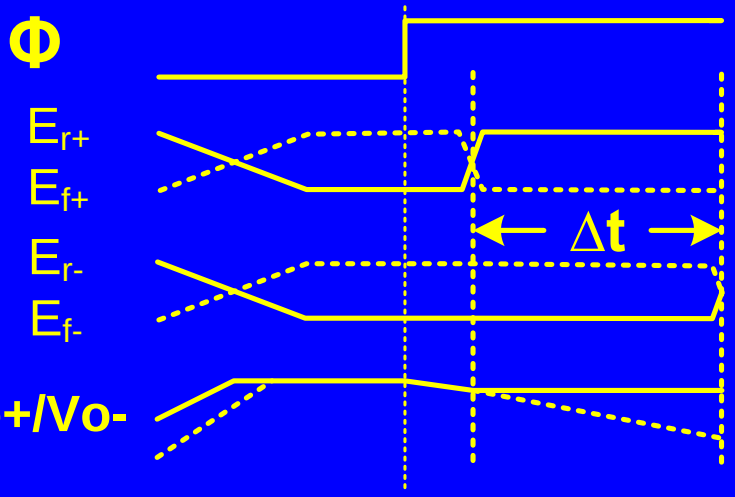
T2V for one tap — evaluation: common pull-down



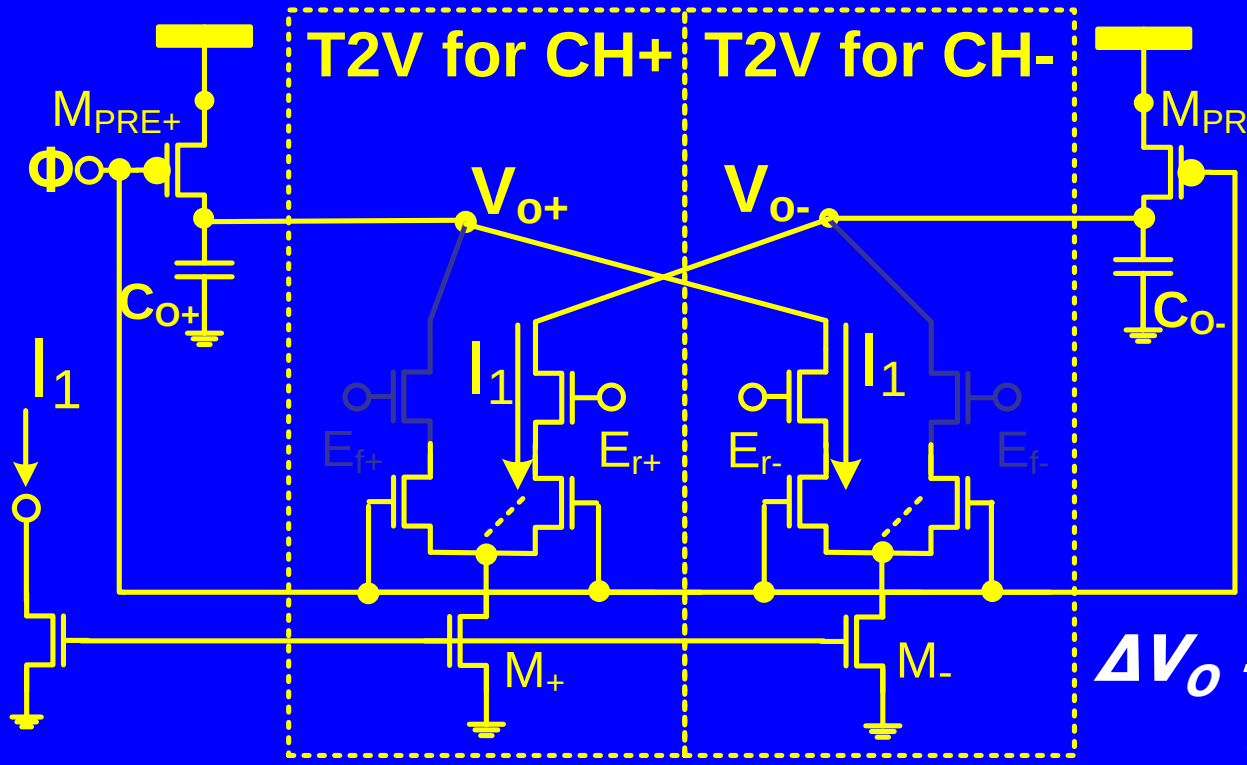


T2V for one tap — evaluation: differentiate

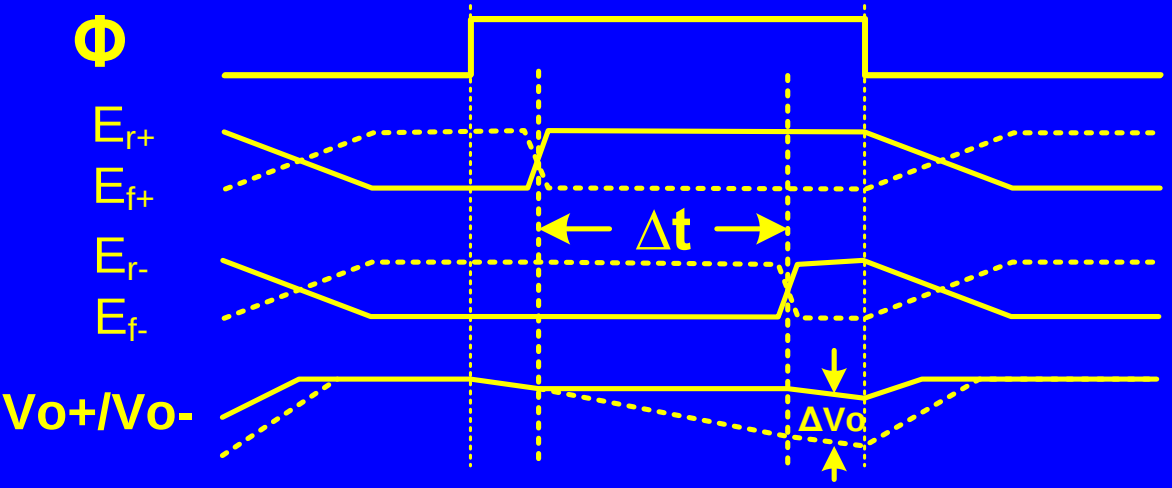




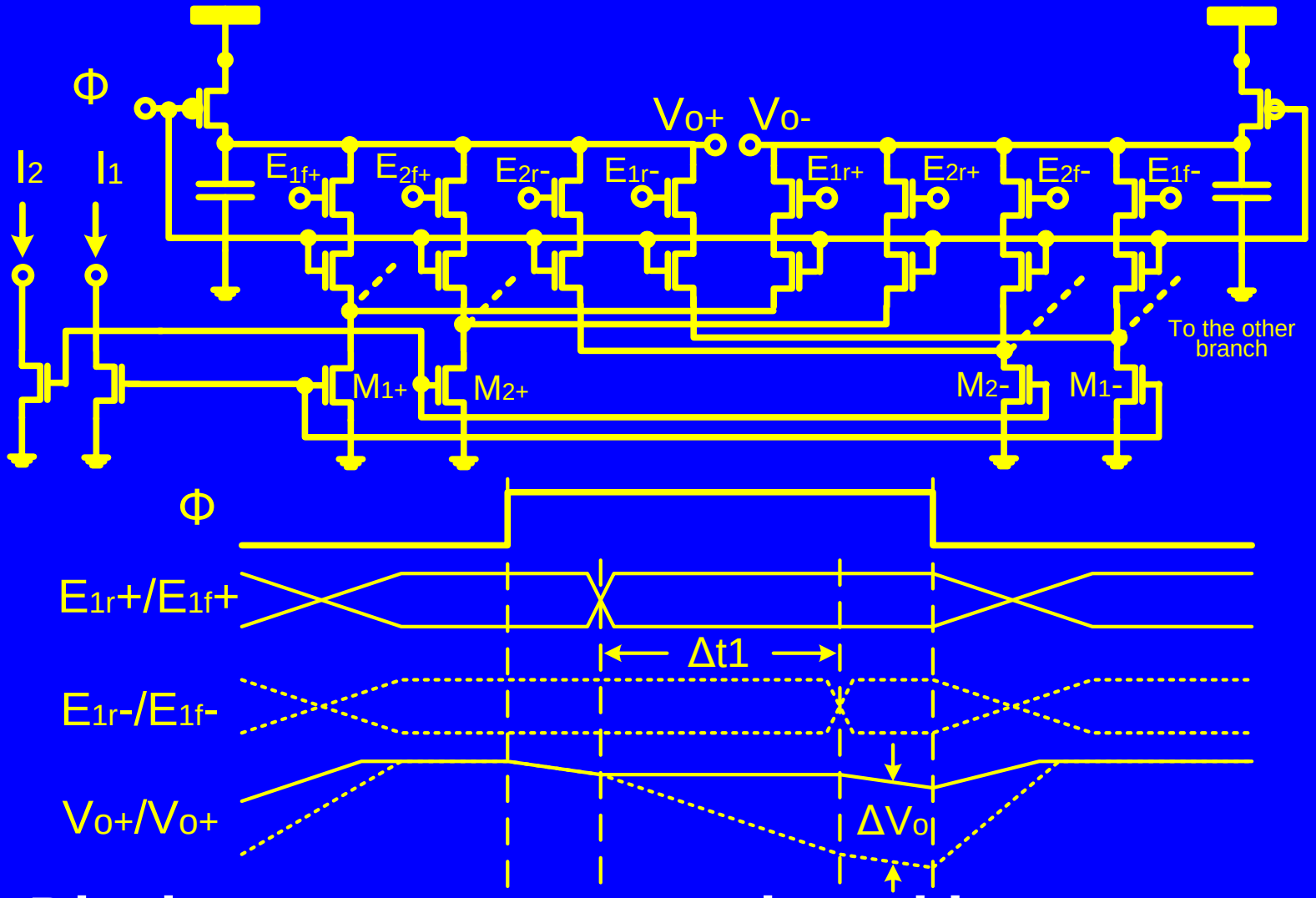
T2V for one tap — evaluation: common pull-down



$$\Delta V_O = \mu \Delta t \, I_1$$
$$= \mu a \Delta V_{in} \, I_1$$

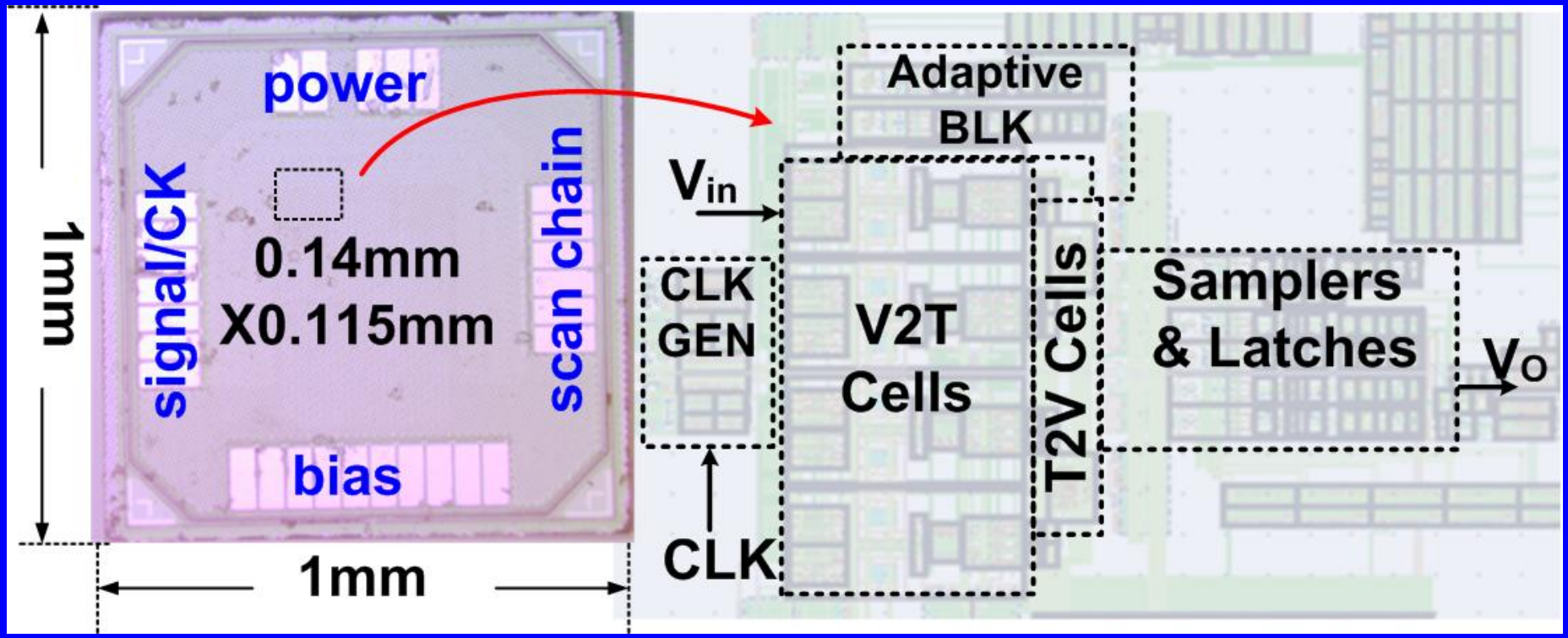


T2V for two taps



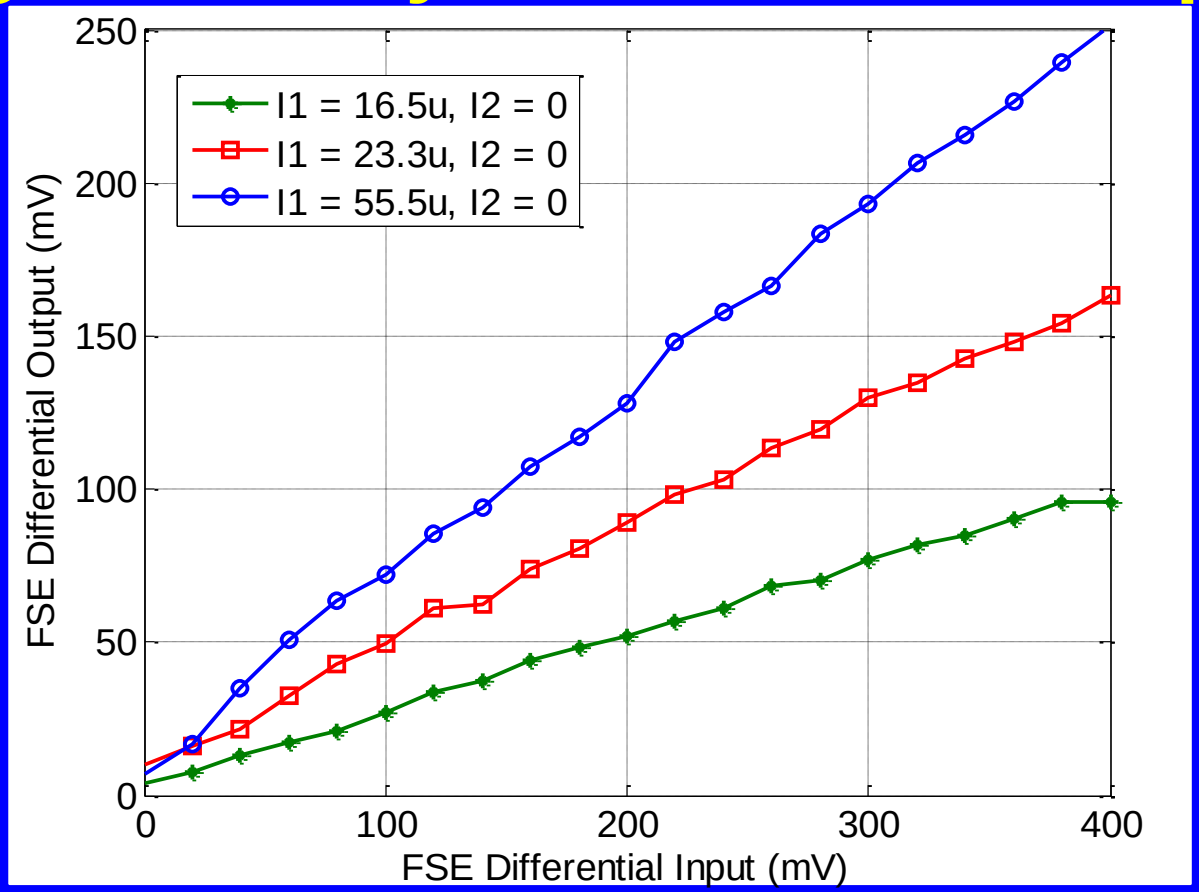
- **Discharge currents are shared between even & odd ways**

Die Photo



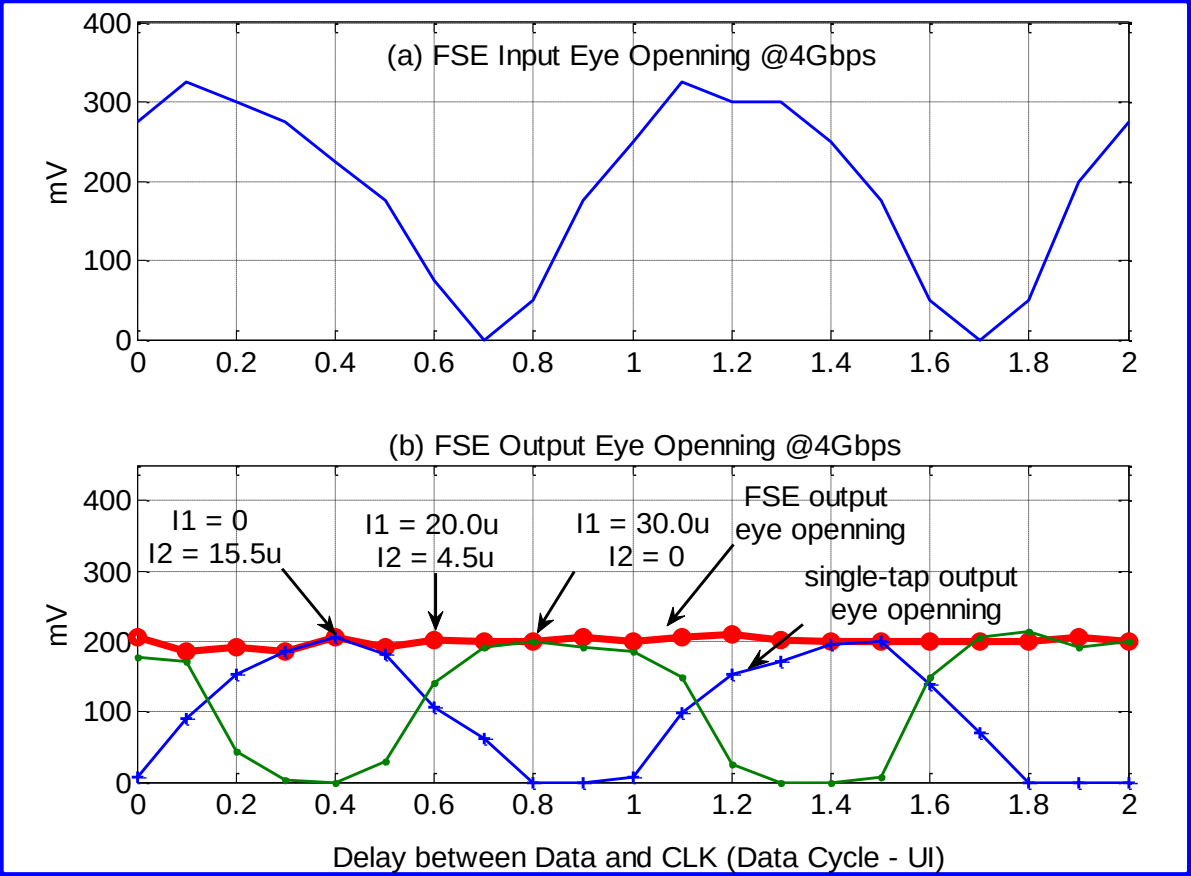
- **Scan-chain/snapshot for in-situ link margin characterization**

Tap weight linearity measured @ 4Gbps rate



- **4.3 effective bits linearity in tap weights**
  - **Monotonic gain**
- **8 mW power consumption w/ 1.2 V supply**
  - **@ 4Gbps**

Phase robustness is shown @ 4Gbps rate



- ±5% eye open variation
  - Gain mismatch of factor 2 between I_1 and I_2
  - Tap weights are tuned

Conclusions

- FSE integrates EQ and phase interpolation
  - Leverage process speed vs. channel BW
- A two-tap FSE receiver is shown
  - Robust against phase offset
  - Voltage-to-time technique scales well compare to CML
    - 4.3 effective bit linearity @ ±400 mv input DR
    - 2 pJ/bit power efficiency @ 4 Gbps

Acknowledgement

- National Semiconductor Corporation
- Center for Integrated Circuits and Systems (CICS) at MIT
- Trusted Foundry for chip fabrication

- Fred Chen