Energy-Delay Tradeoffs in Combinational Logic using Gate Sizing and Supply Voltage Optimization

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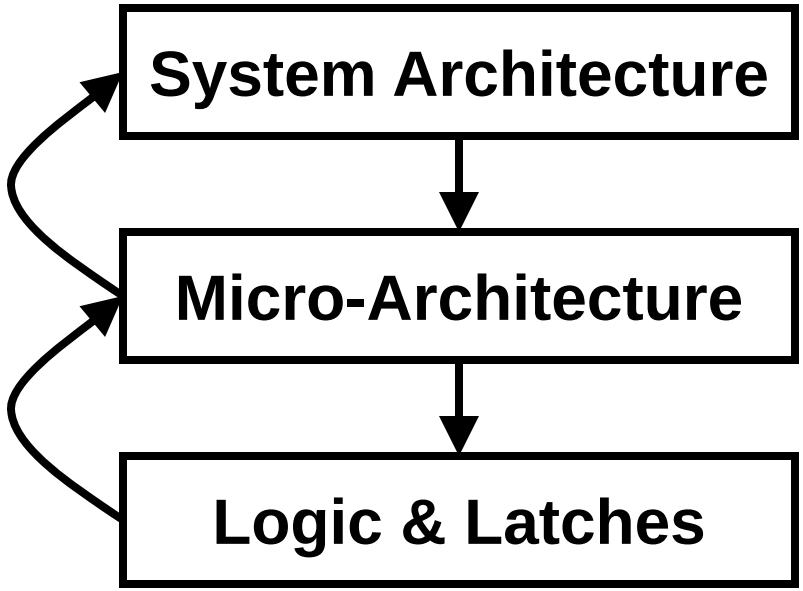
Outline

- Introduction
- Delay and Energy Models
- Circuit Examples
- Optimization Results
- Conclusions

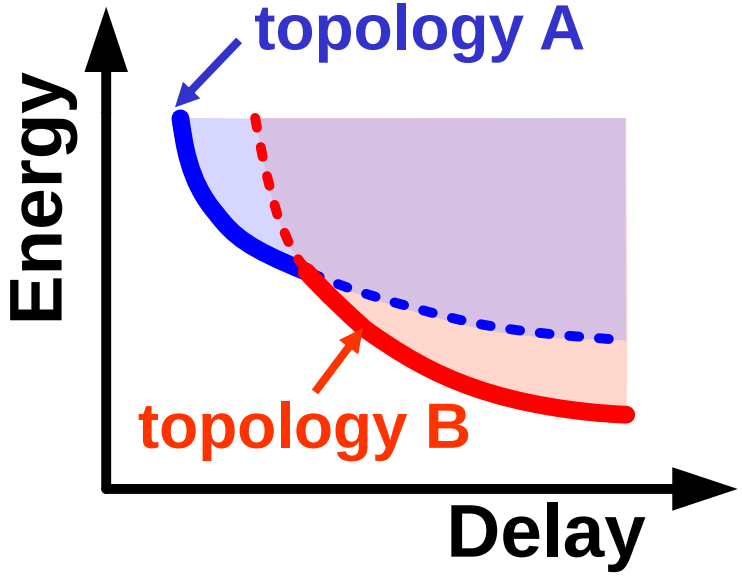
Introduction

- Maximize throughput for a given energy
- Minimize energy for a given throughput



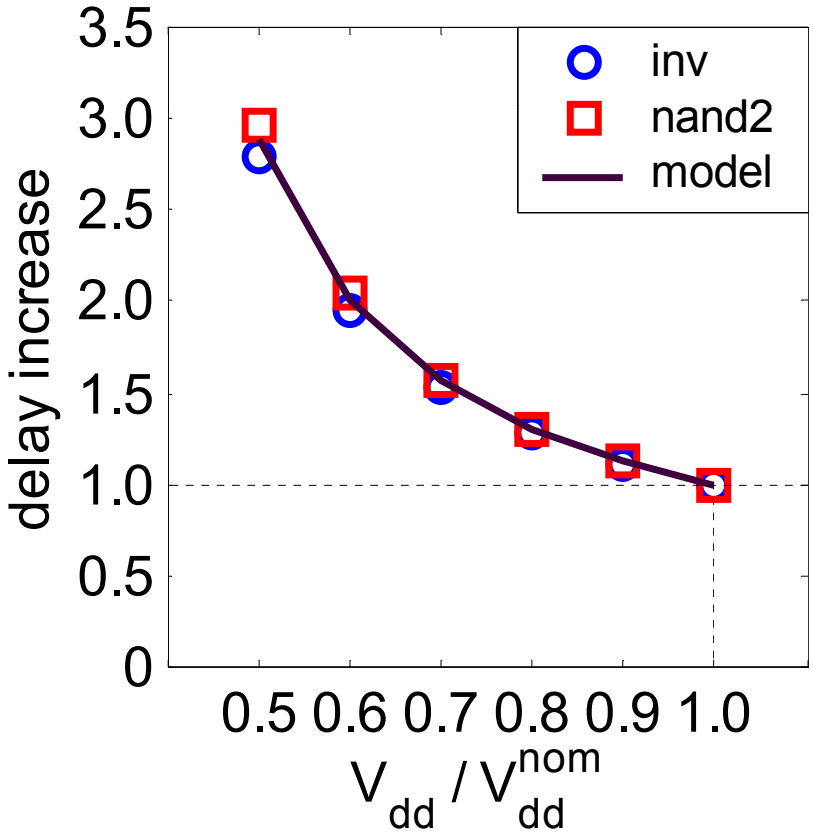
Circuit Optimization

- Boundary curve indicates the best energy-delay tradeoff
- Tuning variables
  - W
  - V_{dd}
- Interesting problems
  - number of V_{dd}'s
  - utilize W or V_{dd}



Alpha-power based Delay Model

$$t_p = \frac{K_d \cdot V_{dd}}{\left(V_{dd} - V_{on}\right)^{\alpha_d}} \cdot \left(\frac{W_{out}}{W_{in}} + \frac{W_{par}}{W_{in}} \right) = \tau_{nom} \cdot g \cdot \left(h + \frac{p}{g} \right)$$

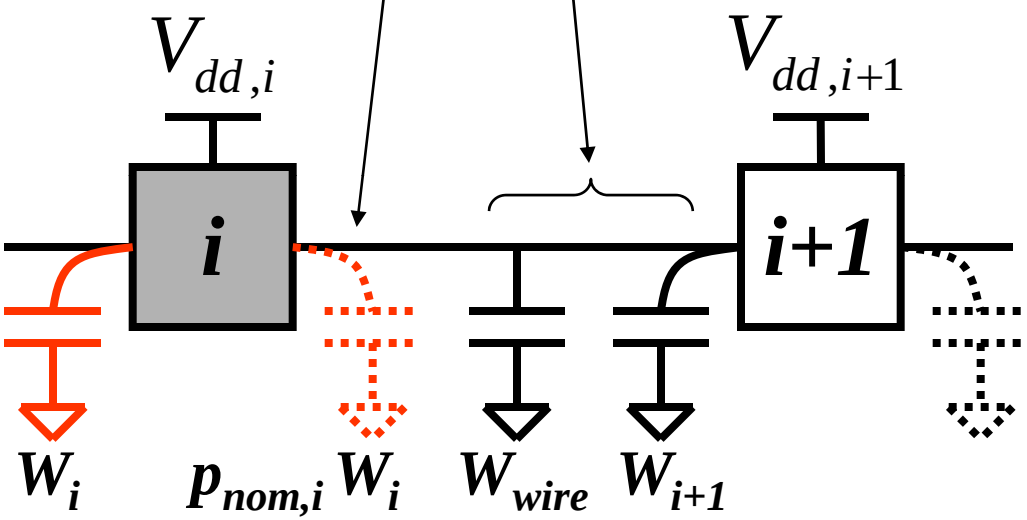


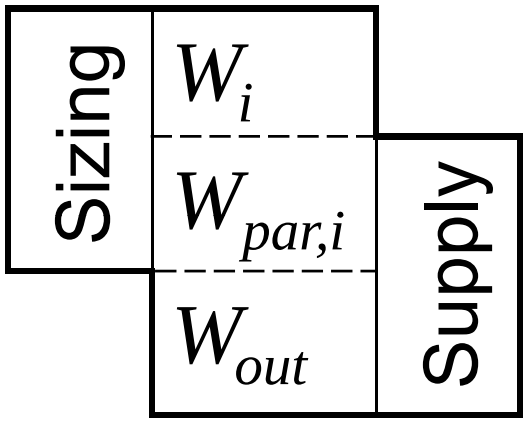
- Fitting parameters V_{on}, α_d, K_d
- Effective fanout

$$h_{eff} = g \cdot h$$

Switching Component of Energy

$$E = K_e \cdot \left(W_{par} + W_{out} \right) \cdot V_{dd}^{\ 2}$$



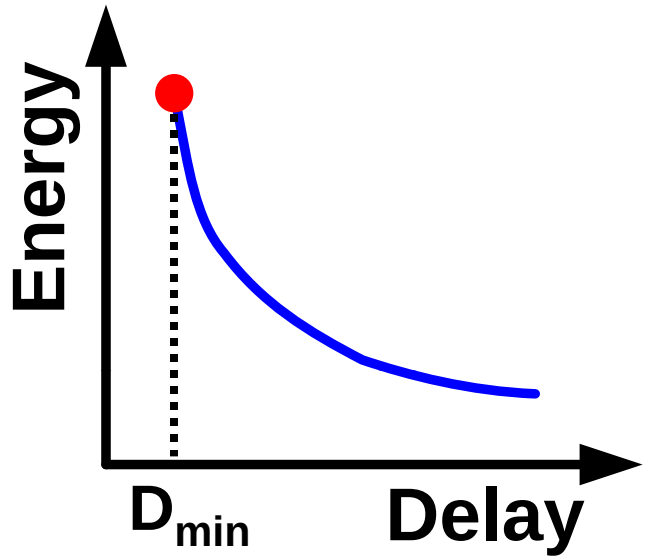


$$ec_i = K_e \cdot W_i \cdot \left(V_{dd,i-1}^{\ 2} + p_{nom,i} \cdot V_{dd,i}^{\ 2} \right)$$

= energy stored on the logic gate *i*

Optimization Setup

- Reference/nominal circuit
  - sized for D_{min} @ V_{dd}^{nom}
- Define delay constraint
  - $D_{con}=D_{min}(1+d_{inc}/100)$



- Minimize energy under delay constraint
  - V_{dd} scaling (global, discrete, per-stage)
  - gate sizing
  - optional buffering

Profitability of Optimization Depends on Sensitivity (∂E/∂D)

- Gate Sizing

$$\frac{\partial E / \partial W_i}{\partial D / \partial W_i} = -\frac{K_e}{K_d} \cdot \frac{ec_i}{h_{eff,i} - h_{eff,i-1}}$$

∞ for equal h_{eff} (D_{min})

- Supply Voltage

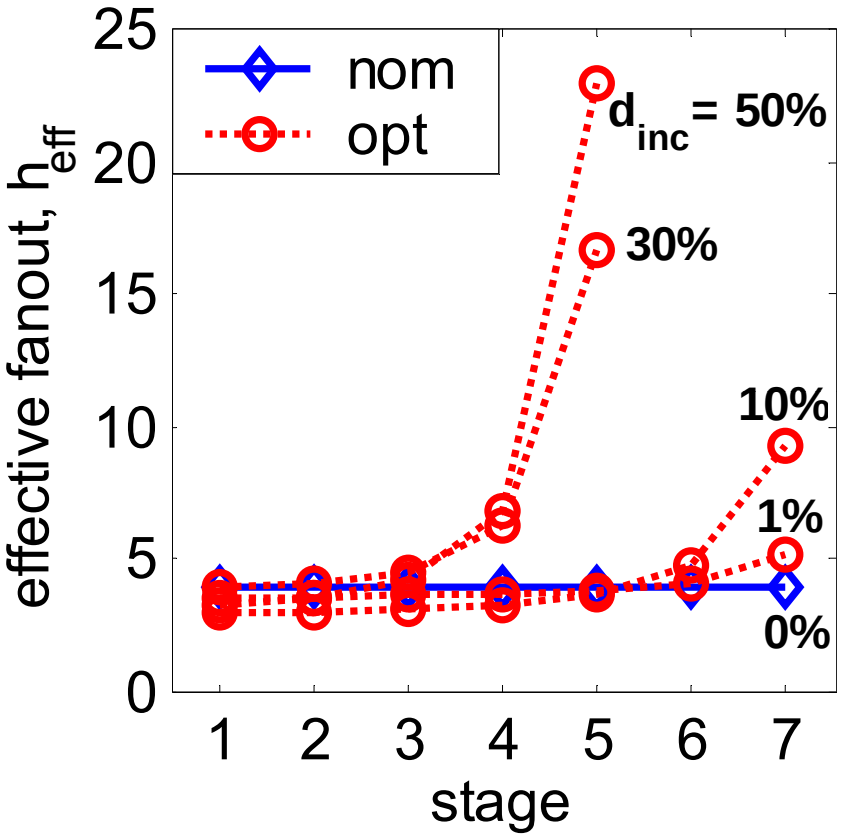
$$\frac{\partial E / \partial V_{dd}}{\partial D / \partial V_{dd}} = -\frac{E}{D} \cdot \frac{2 \cdot \left(1 - \frac{V_{on}}{V_{dd}}\right)}{\alpha_d - 1 + \frac{V_{on}}{V_{dd}}}$$

max at D_{min}

Circuit Examples

- Inverter chain
  - No off-path load or reconvergence
- Memory decoder
  - Off-path load without reconvergence
- Adder
  - Off-path load with reconvergence

Inverter Chain: Sizing Optimization



$$W_i^2 = \frac{W_{i-1} \cdot W_{i+1}}{1 + \mu \cdot W_{i-1}}$$

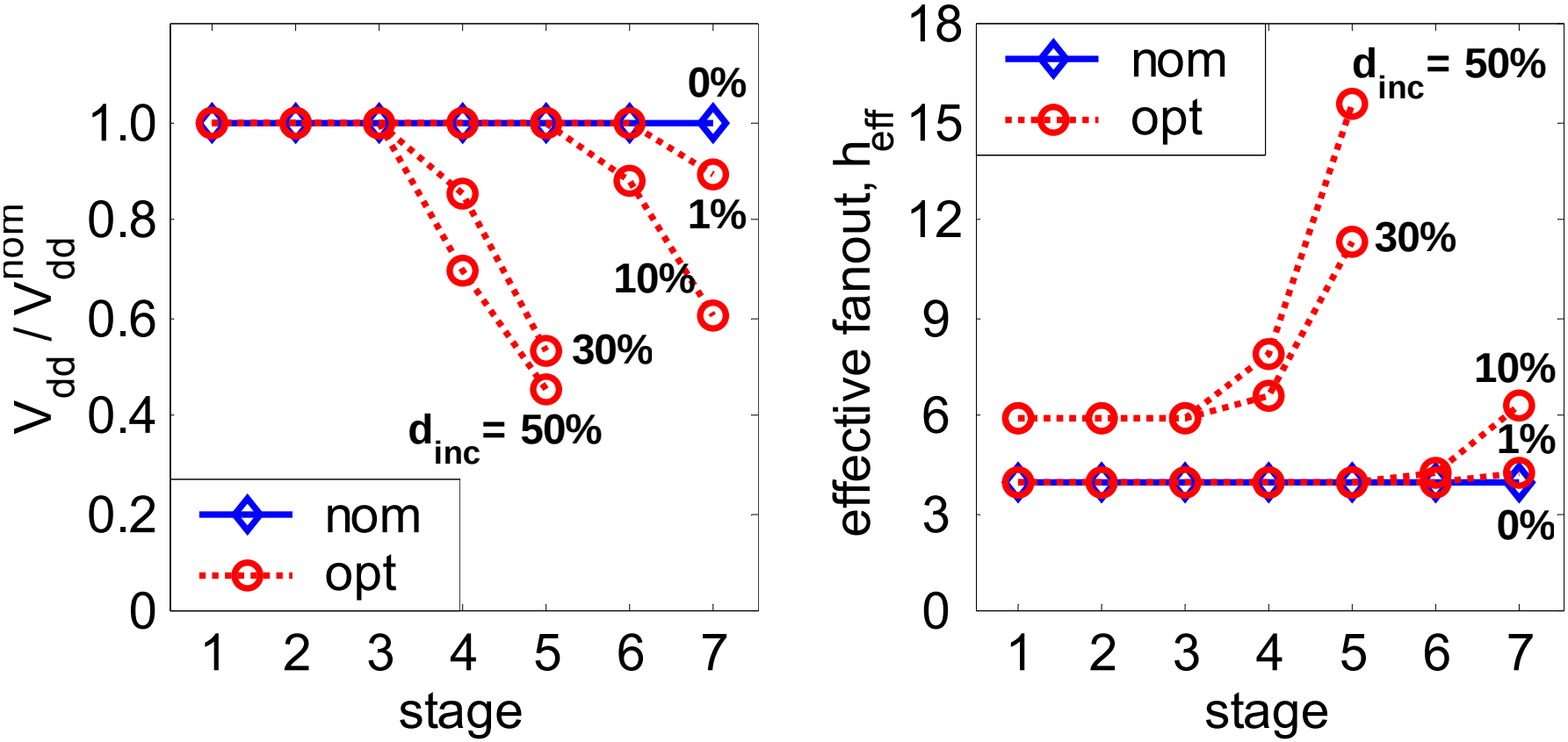
[Ma, Franzon, *IEEE JSSC*, 9/94]

$$\mu = -\frac{2 \cdot K_e \cdot V_{dd}^2}{\tau_{nom} \cdot S_W}$$

$$S_W \propto \frac{ec_i}{h_{eff,i} - h_{eff,i-1}}$$

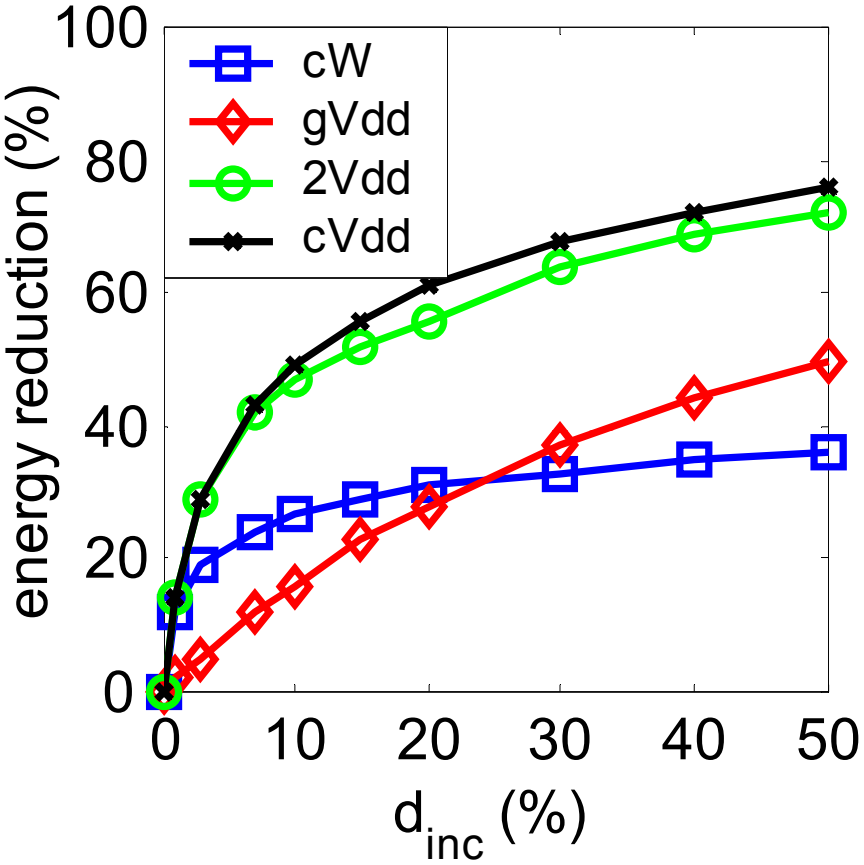
- Variable taper achieves minimum energy
- Reduce number of stages at large d_{inc}

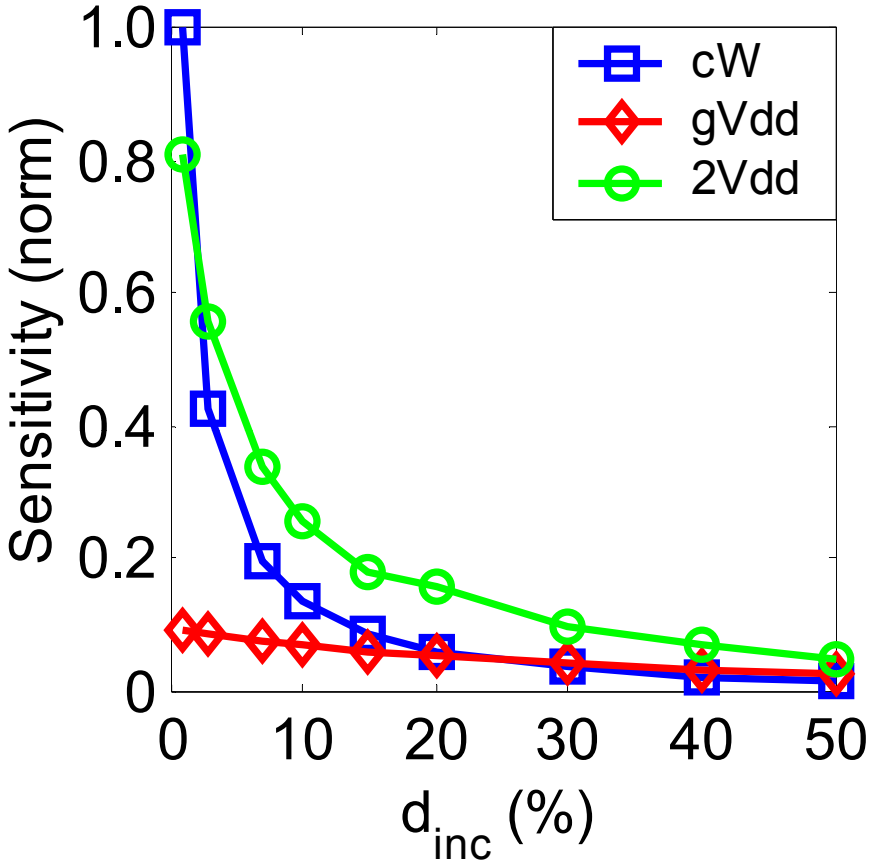
Inverter Chain: Vdd Optimization



- Variable taper achieved by voltage scaling
- V_{dd} reduces energy of the final load first

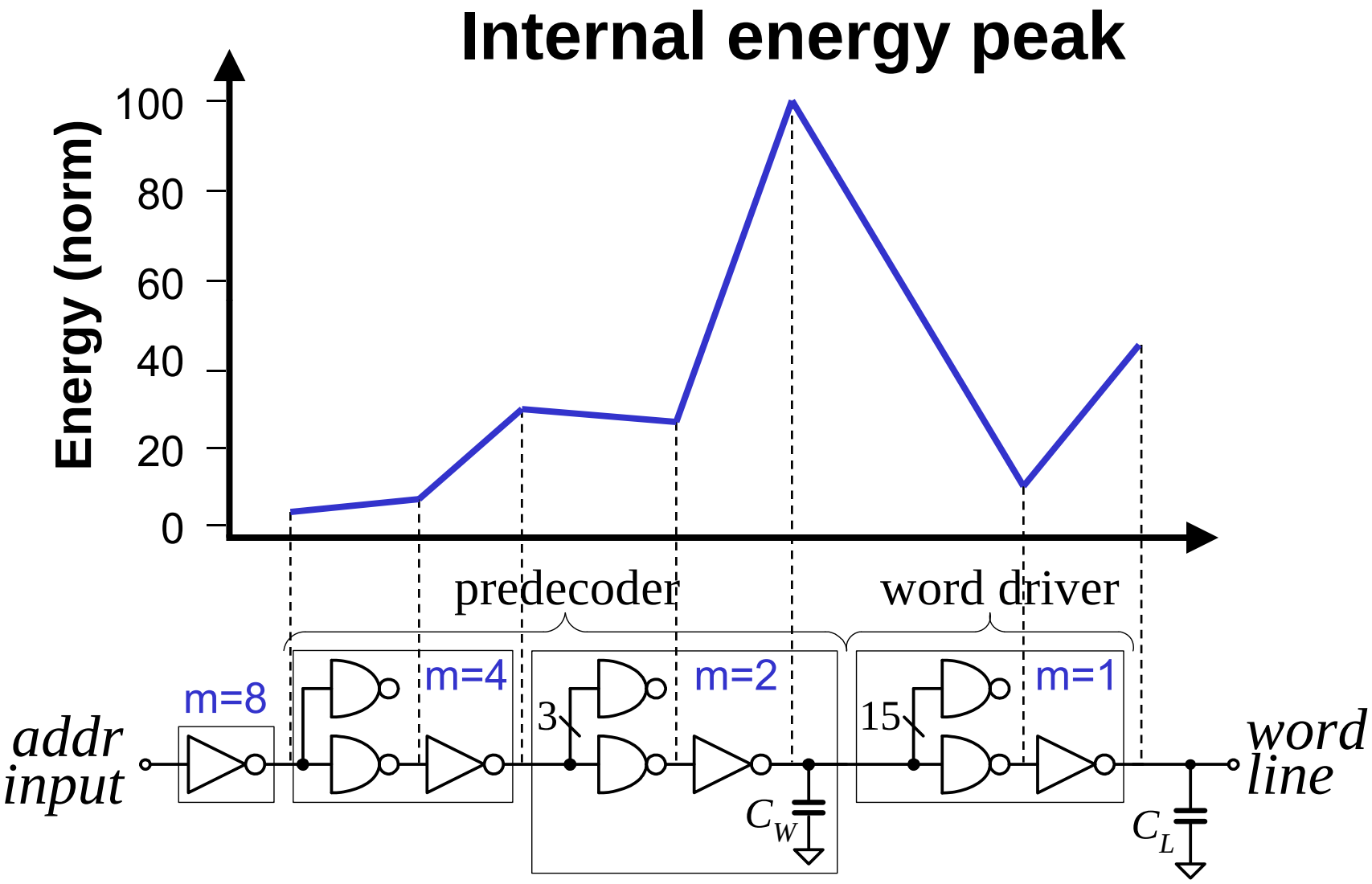
Inverter Chain: Optimization Results



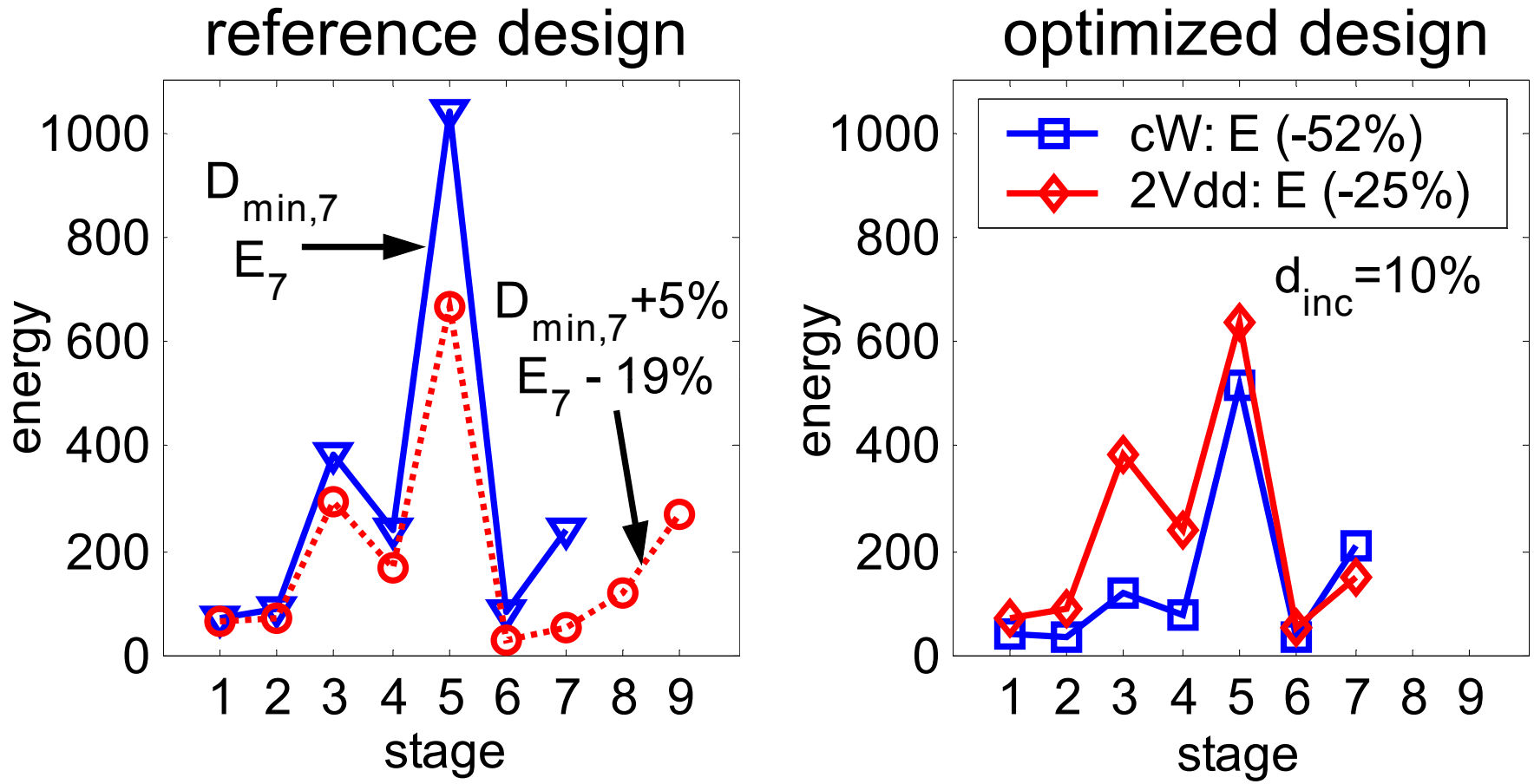


- Parameter with the largest sensitivity has the largest potential for energy reduction
- Two discrete supplies mimic per-stage V_{dd}

SRAM Decoder Energy Profile



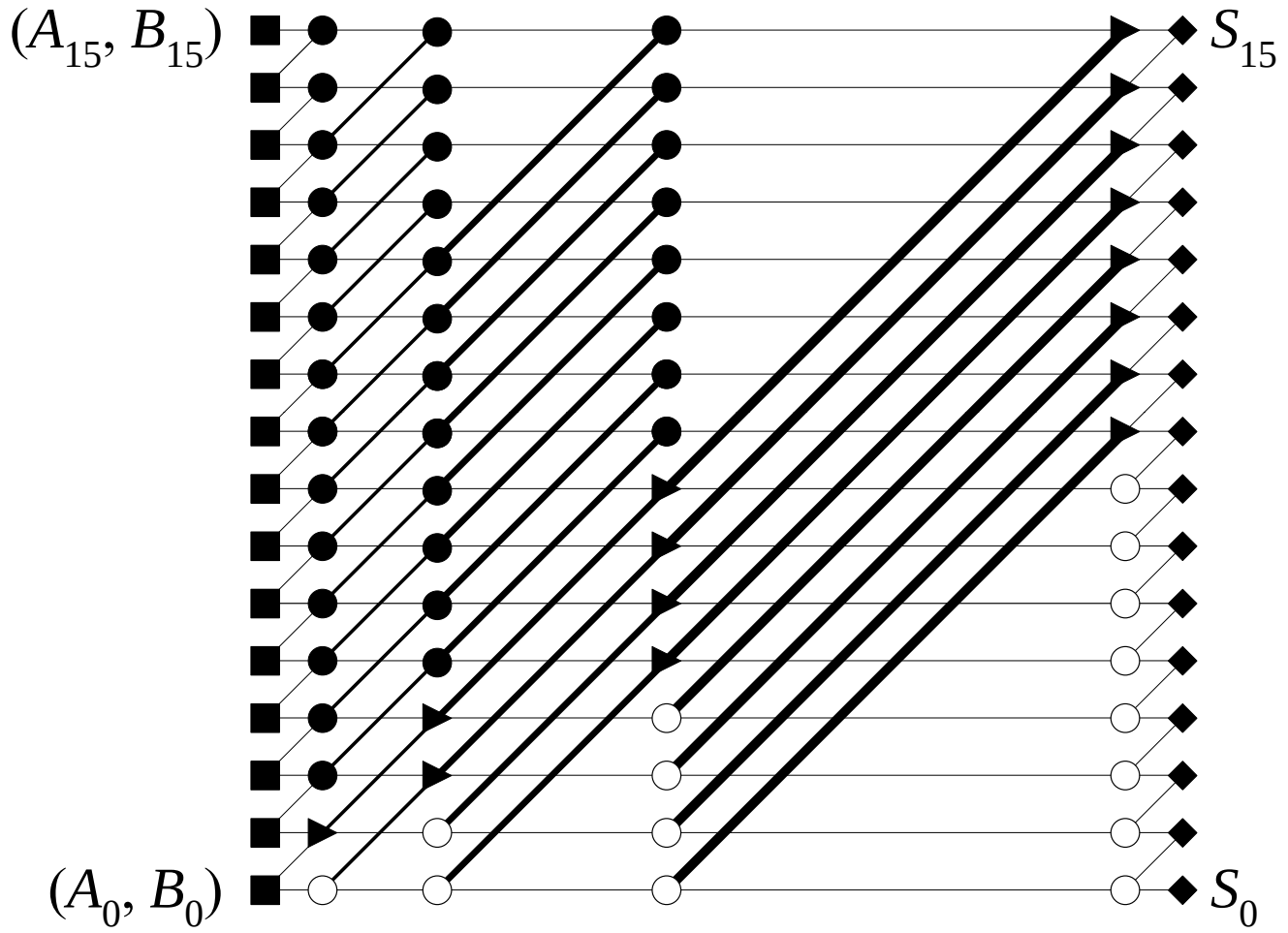
W vs. Vdd for Reducing Energy Peak



- V_{dd} less effective than W optimization
- Buffering also reduces energy peak

[B. Amrutur, *Ph.D. Thesis, Stanford*, 8/99]

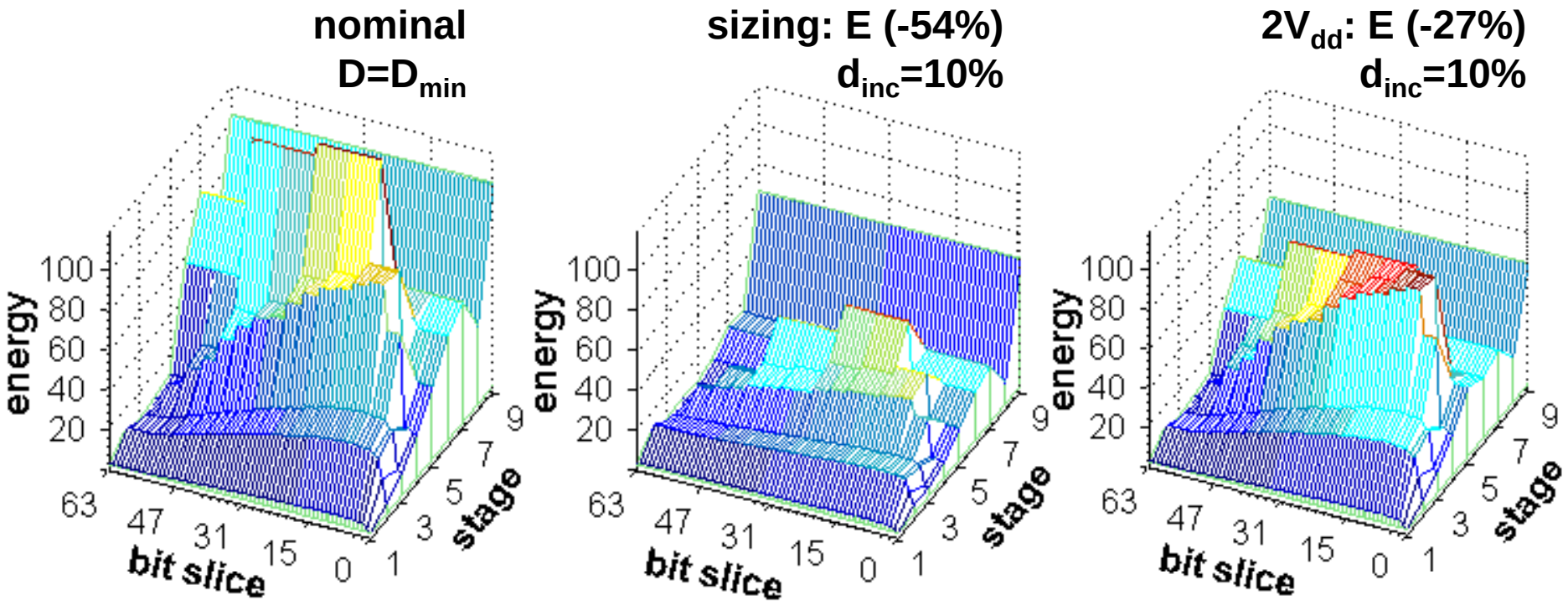
Kogge-Stone Tree Adder Topology



- Off-path load (gates + wires)
- Reconvergence (inside ●-block)

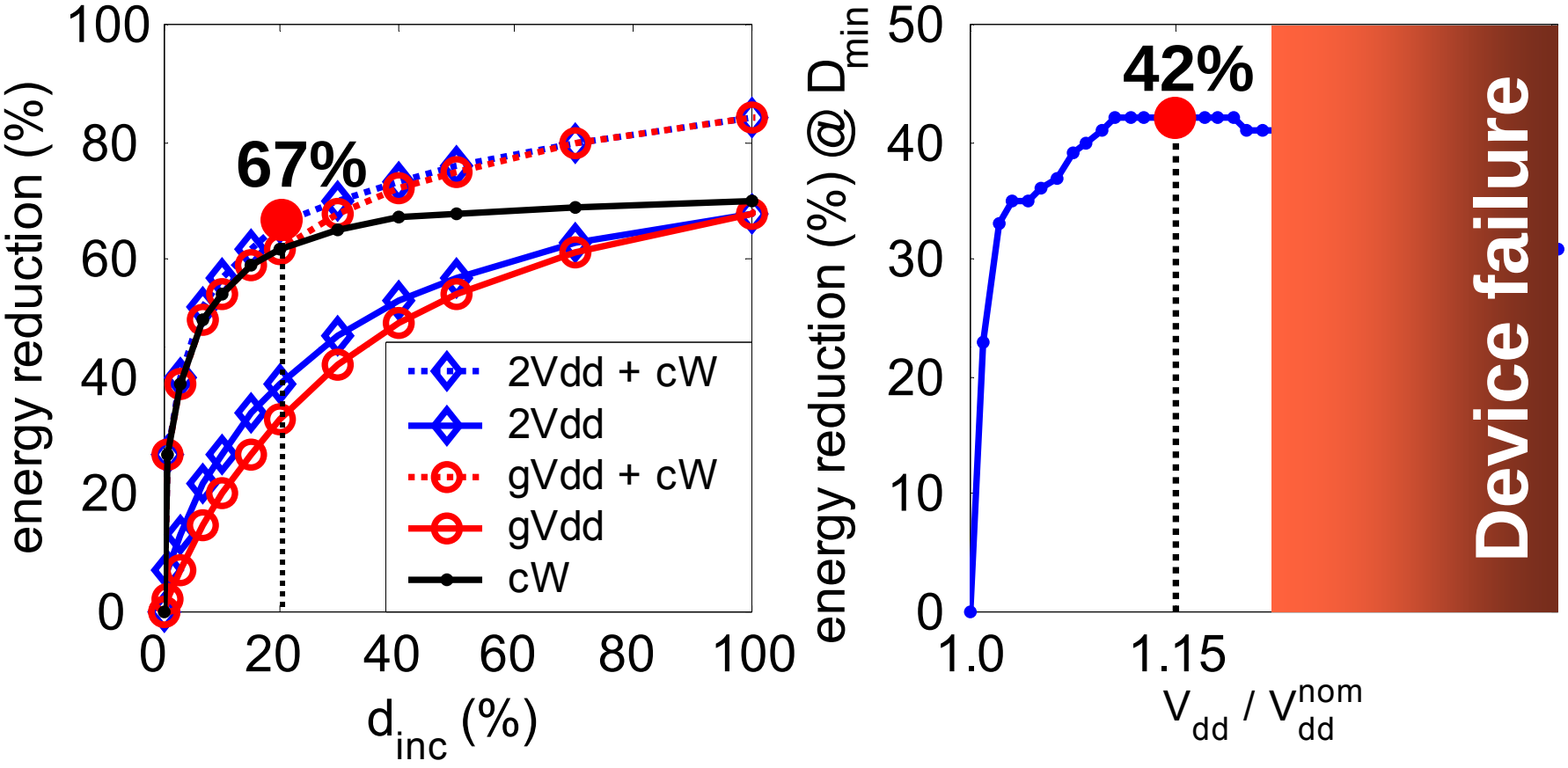
Tree Adder: Optimization Results

- Reference: all paths are critical



- Internal energy $\Rightarrow$ W more effective than V_{dd}
  - W: E(-54%), $2V_{dd}$: E(-27%) at d_{inc}=10%

Tree Adder: Joint Optimization



- Choose a more efficient variable
- Power vs. reliability limit on V_{dd}^{nom}

Conclusions

- A unified optimization framework for energy-efficient design has been demonstrated
- Results
  - Sizing is the most effective for small delay increments while V_{dd} is better for large increments
  - No advantage in more than two supplies for improving energy
  - Sizing and supply optimization can provide up to a 70% energy savings with only a 20% delay penalty