Scaling with photonics inside processors and memory

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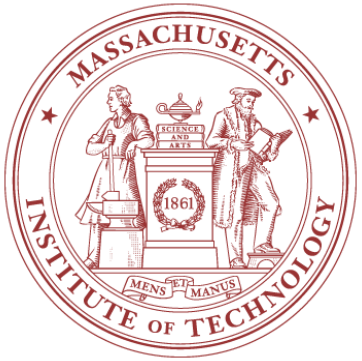
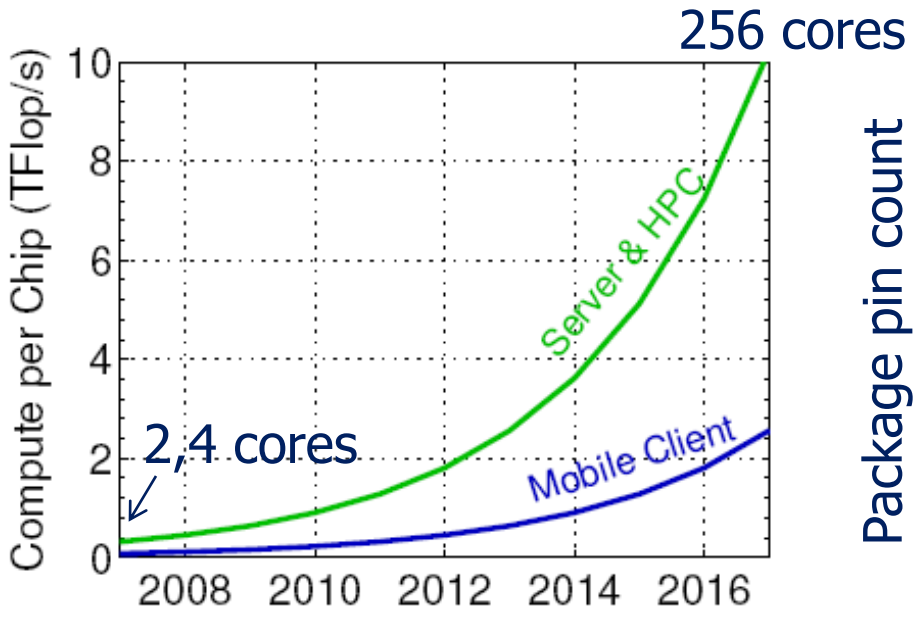
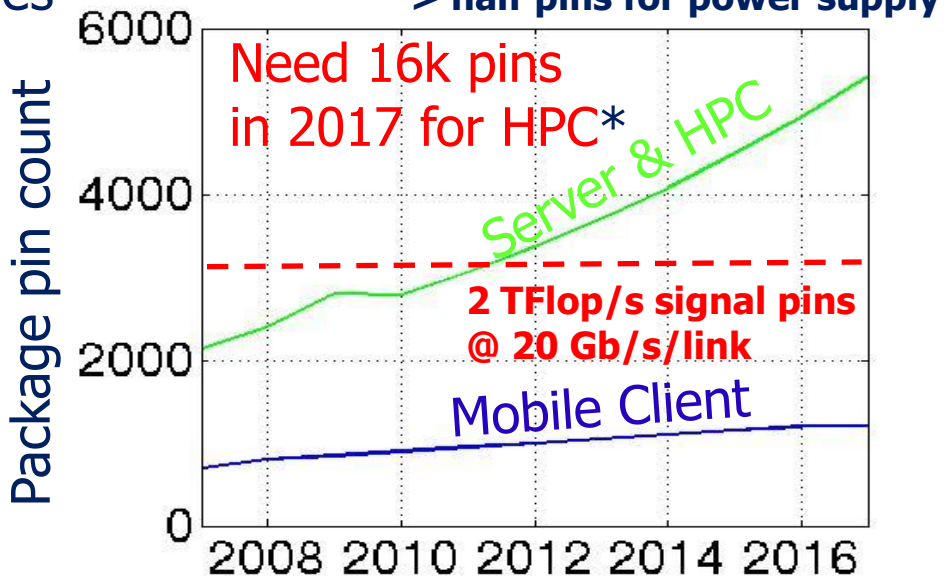
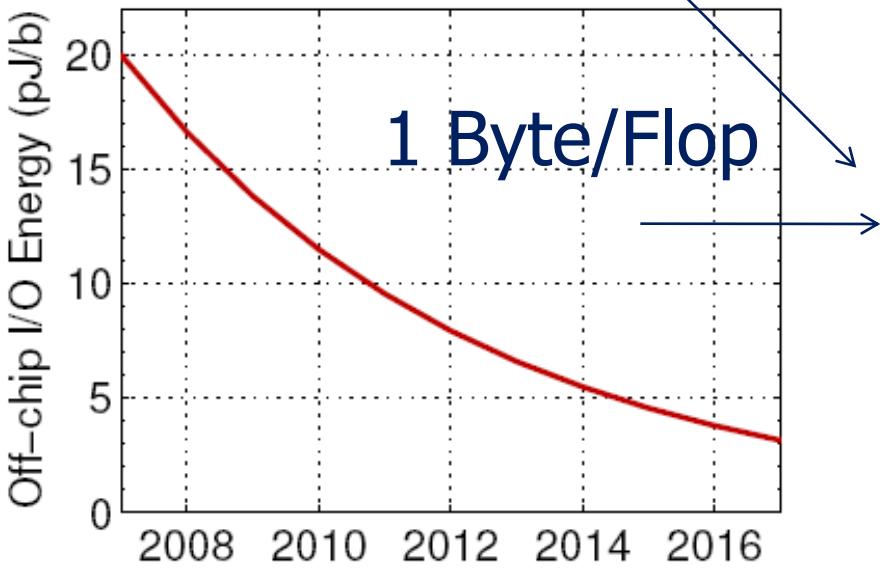
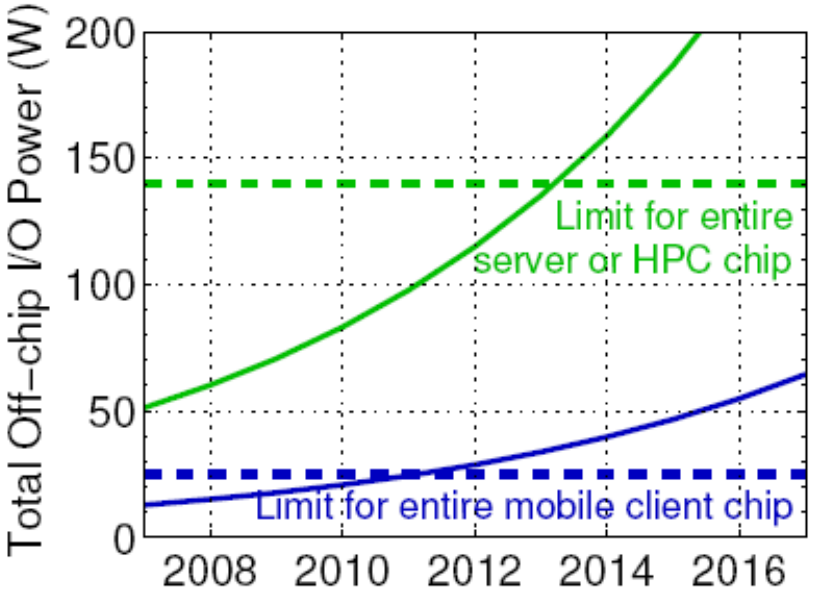


Socket bandwidth, pin count and power scaling

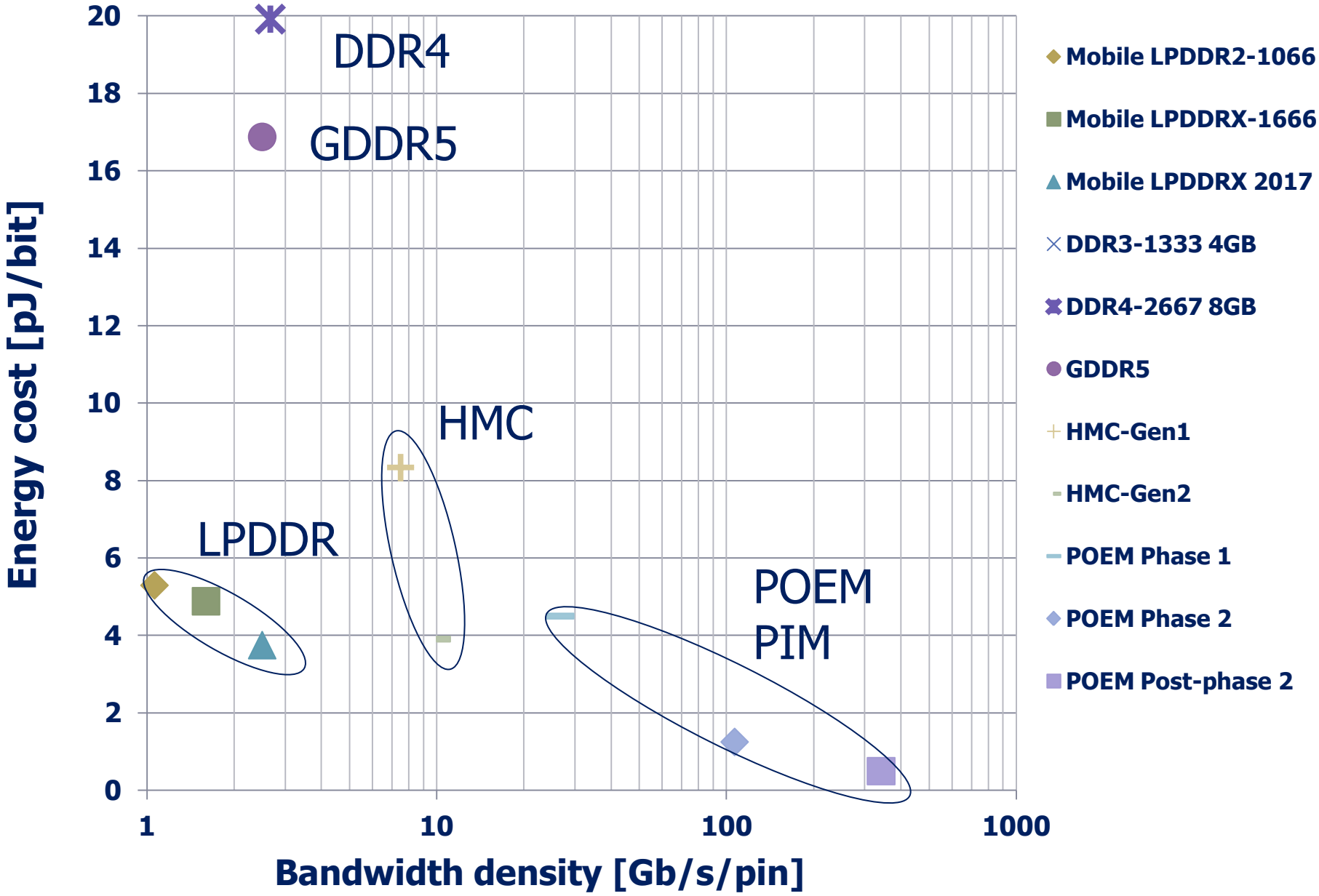




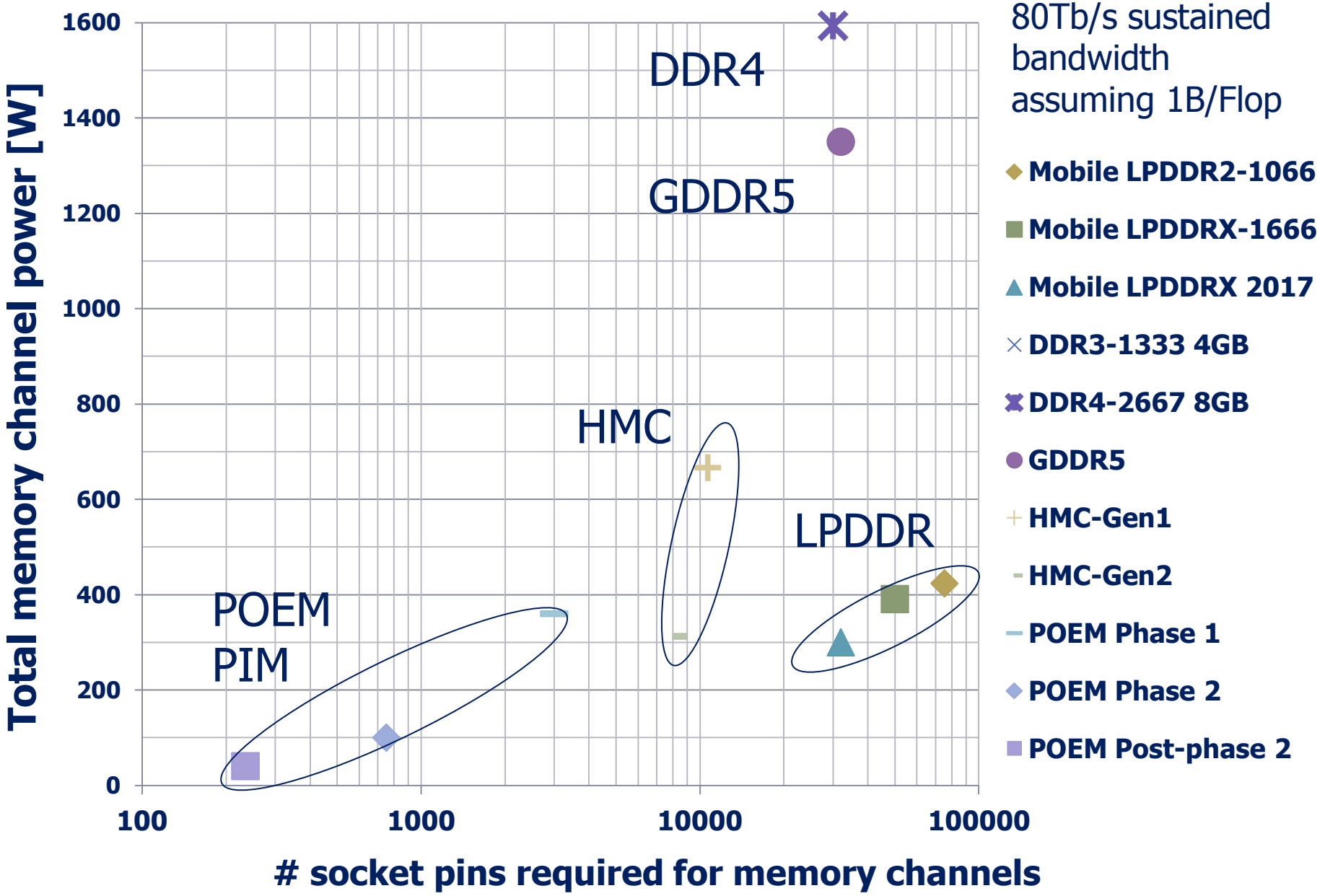




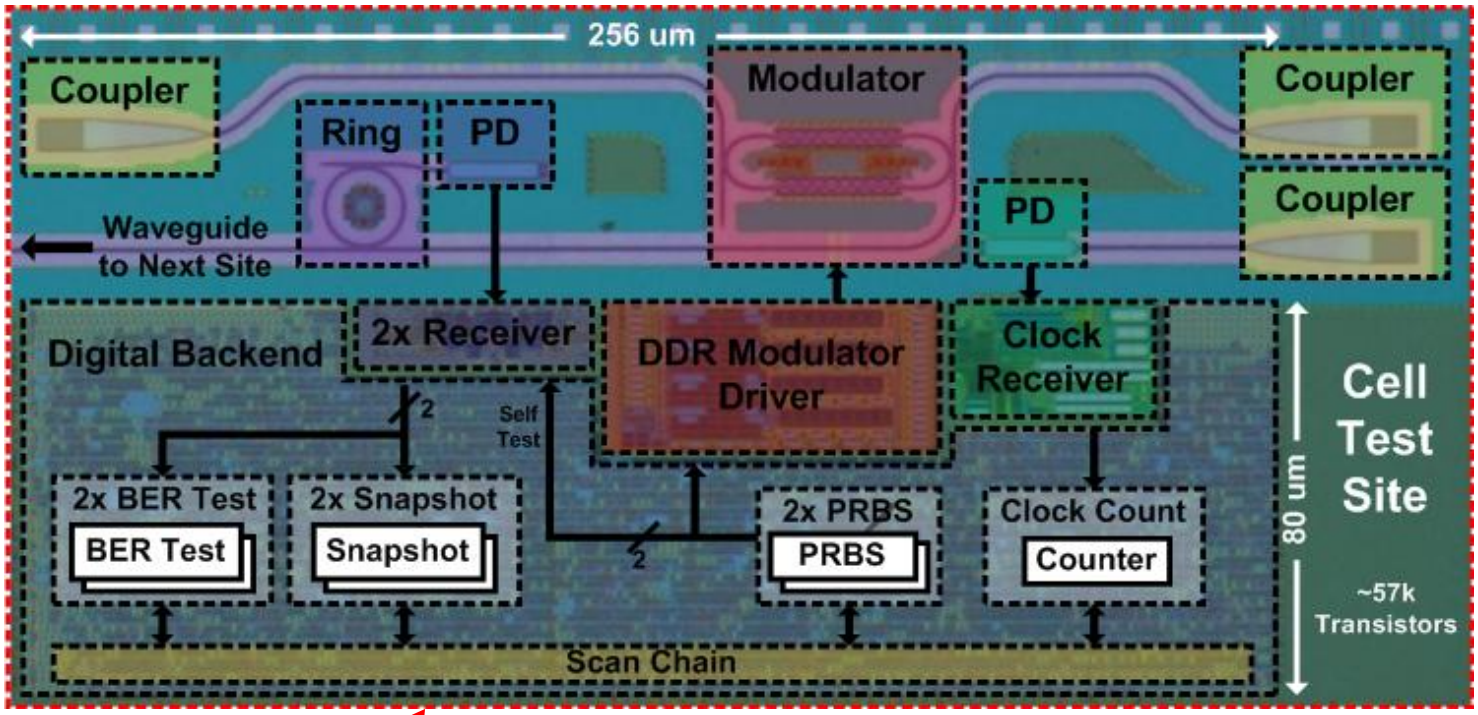
Memory interface scaling problems: Energy-cost and bandwidth density

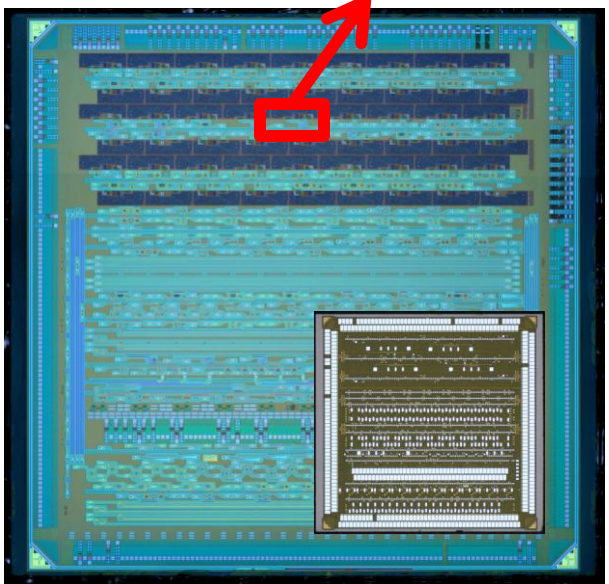


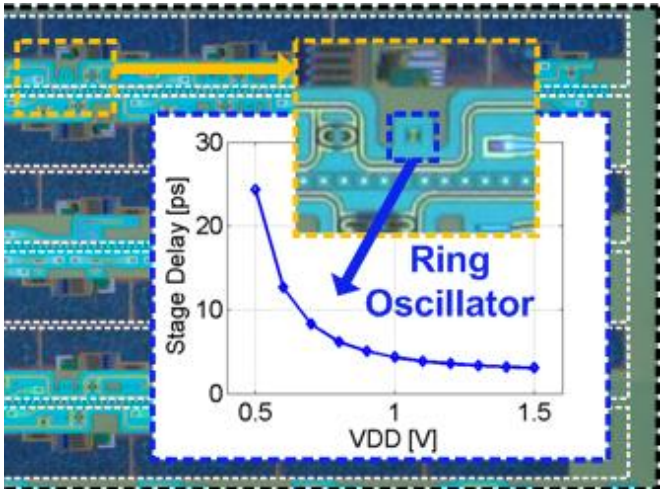
Power and pins required for 10TFlop/s



Photonic links inside CPU chips







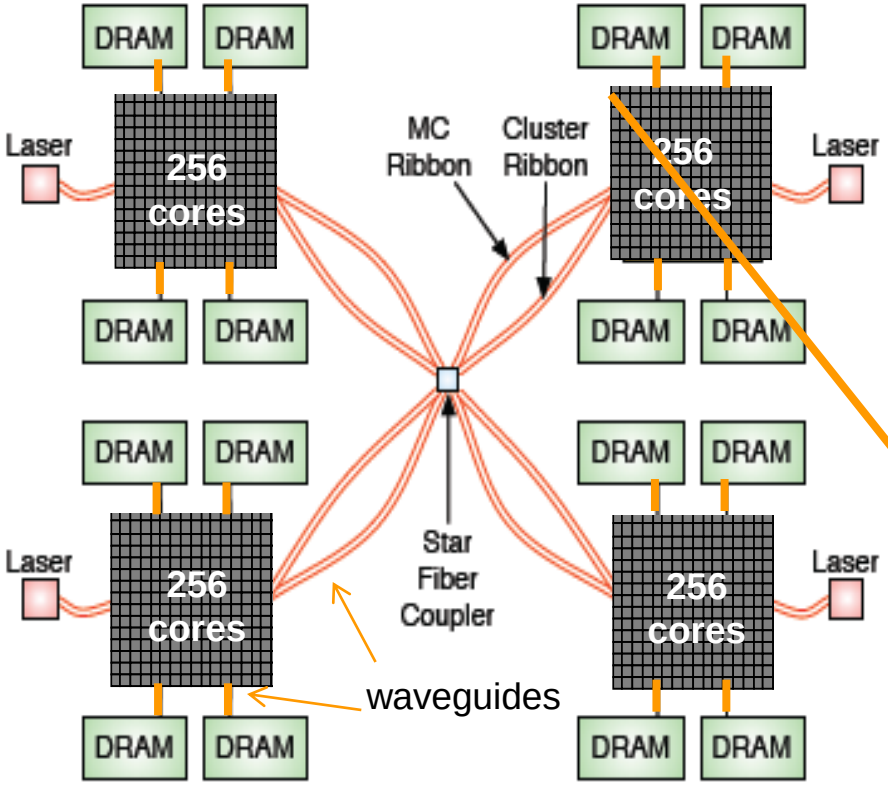
45nm SOI

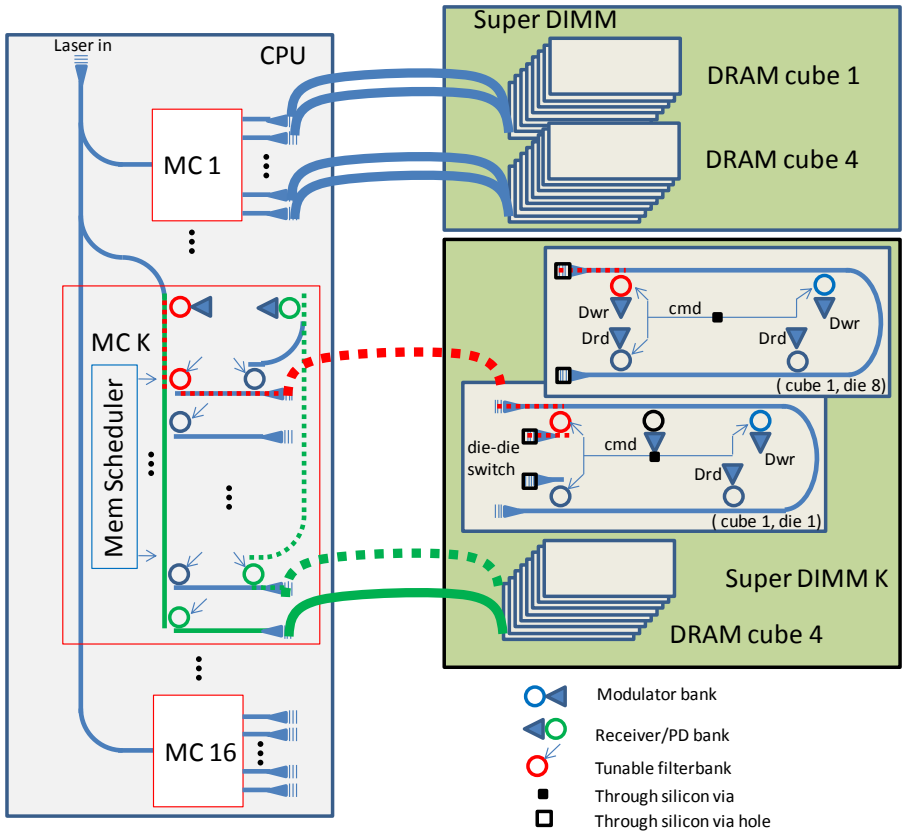
MIT EOS Platform: Stojanovic, Ram, Popovic

10TFlop/s 4-socket node with photonics

Photonic coherency links
- CPU power limited multi-socket

Photonic memory interfaces
- Breaks capacity/throughput bottleneck





Photonically Interconnected Memory
- Laser power guiding from MC
- Photonics inside DRAM stack

[Beamer ISCA 2010, ICS 2009]

Embedded Node Performance