An Overview of Relay Integrated Circuits and Technology

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in collaboration with

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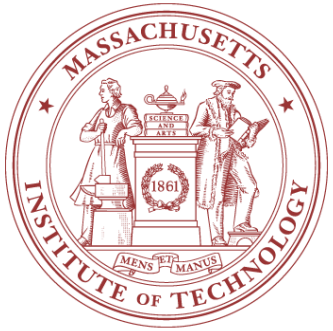
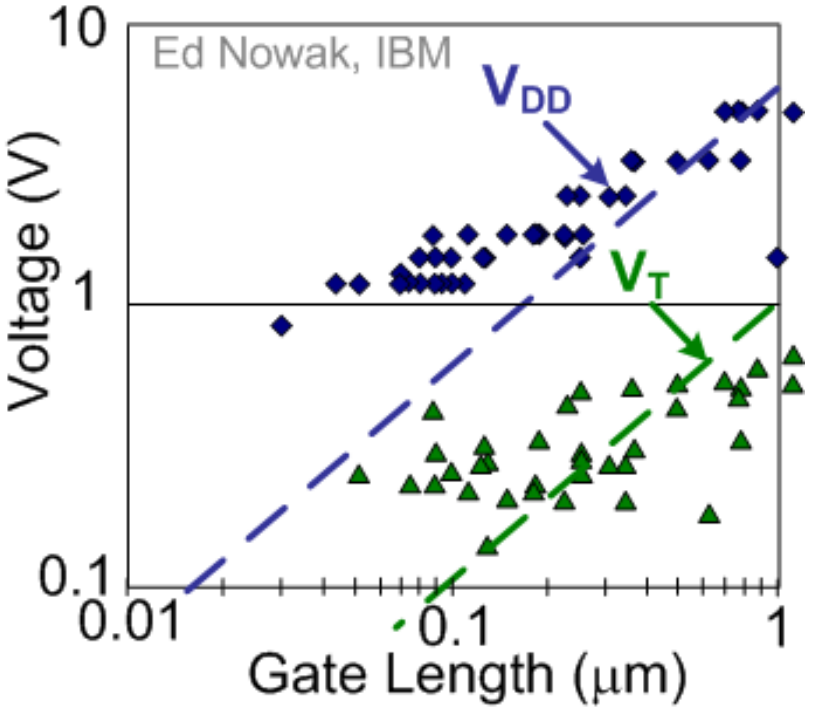
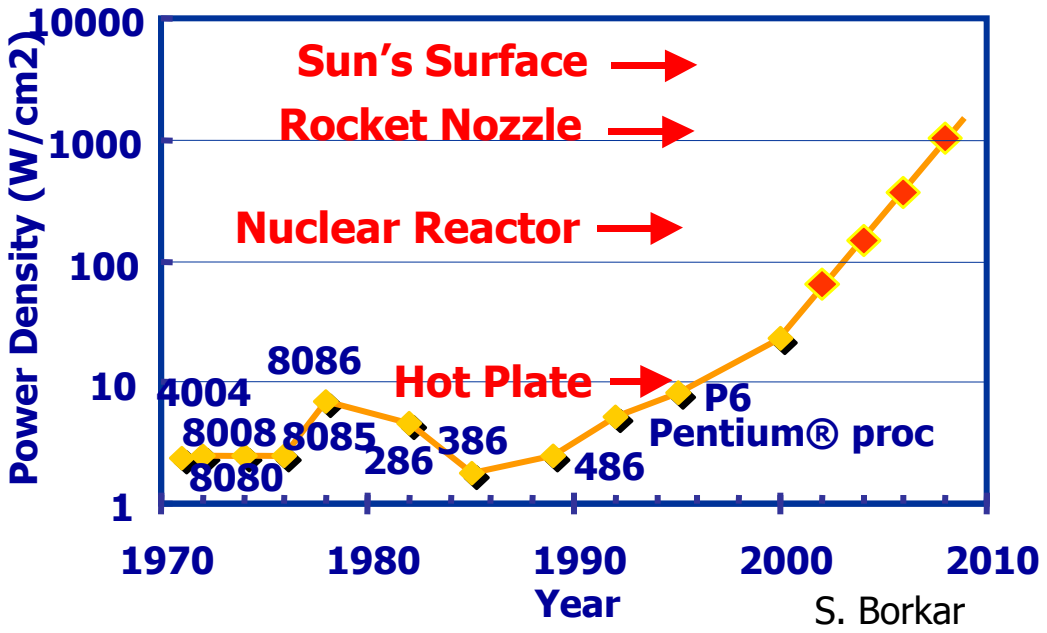


Digital Computing Power Crisis

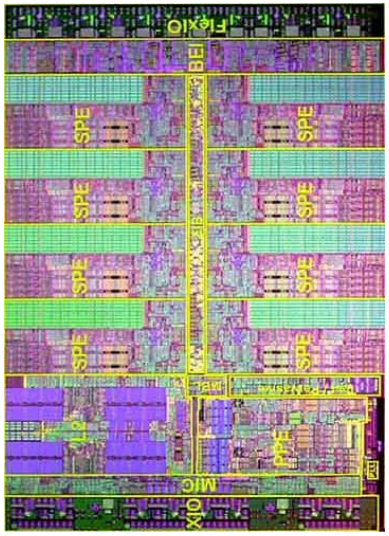


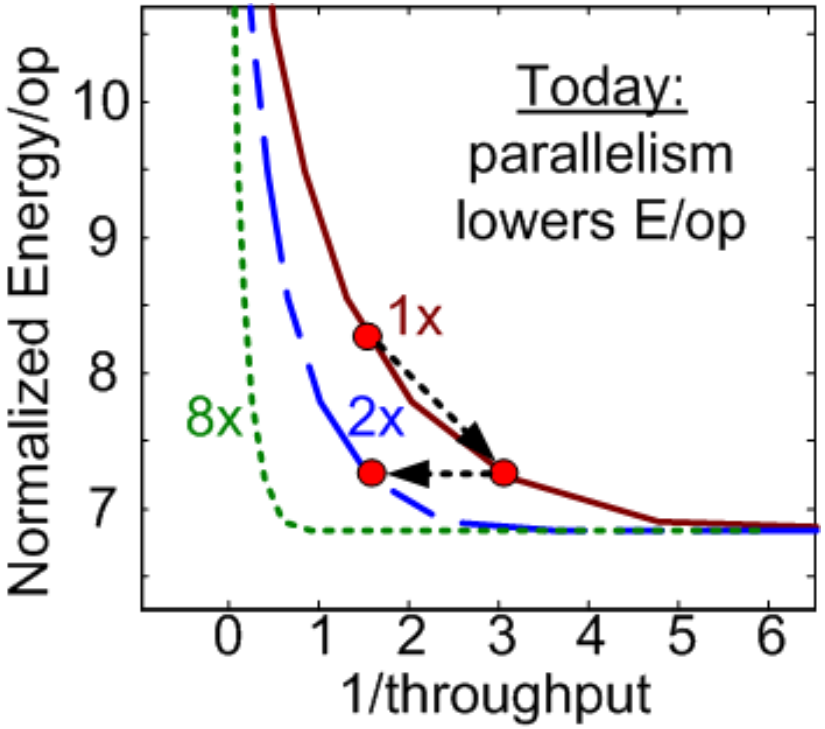
Power Density Prediction circa 2000



- **Since ~2000 supply voltages (V_{DD}) stuck at ~1V**
  - Leakage stops you from lowering threshold (V_T)
- **Leads to very poor power scaling… 1kW chips?**

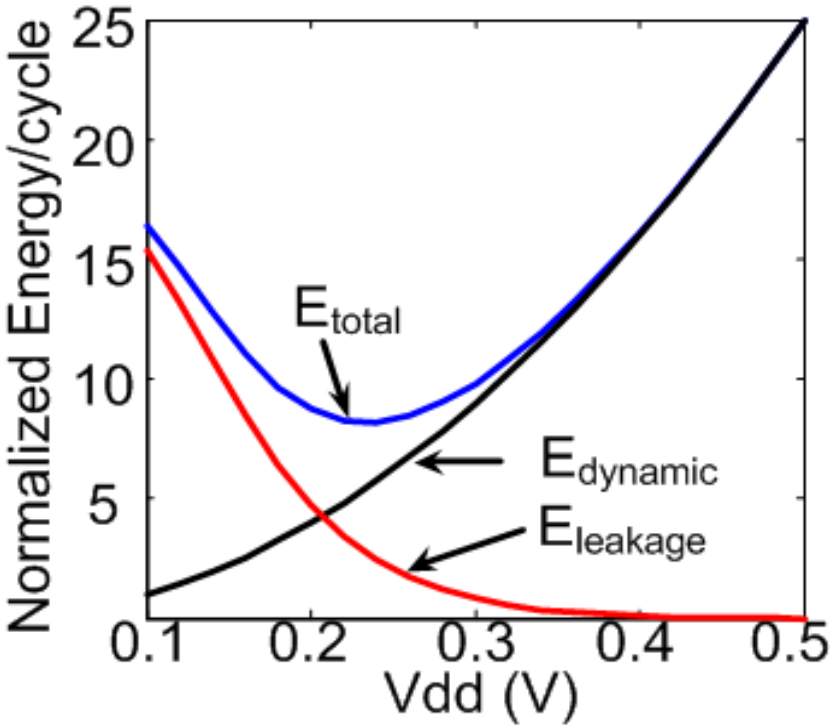
Parallelism to the Rescue

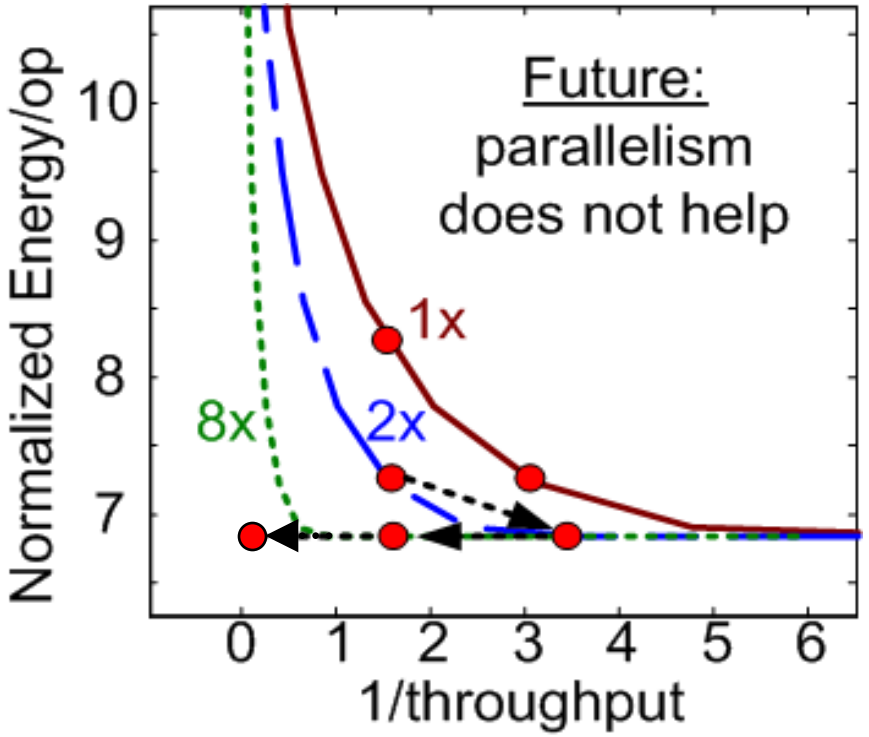




- **Parallelism allows slower, more efficient cores**
  - While maintaining overall throughput
- **Works well (if you can parallel program), but…**

Leakage: Game Over for CMOS

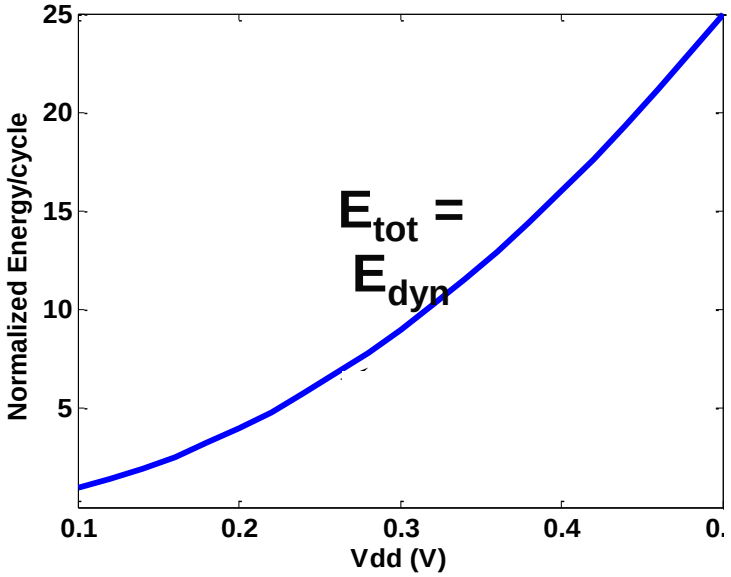




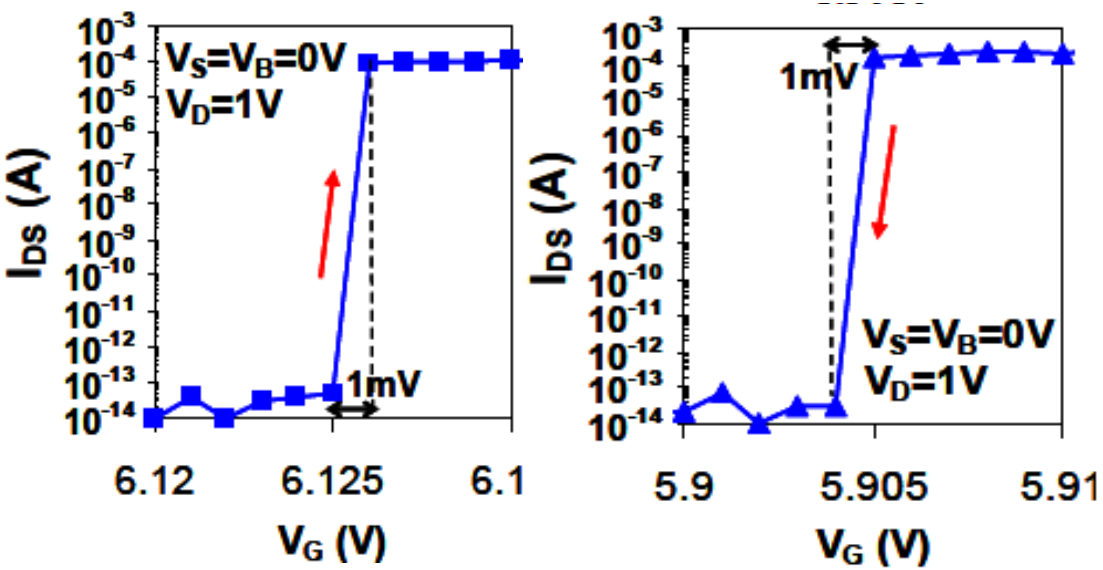
- **CMOS circuits have an absolute minimum energy**
  - Need to balance leakage and dynamic components
- **Parallelism doesn't help if already at E_{min}…**

Relays To The Rescue?

Energy/op vs. Vdd



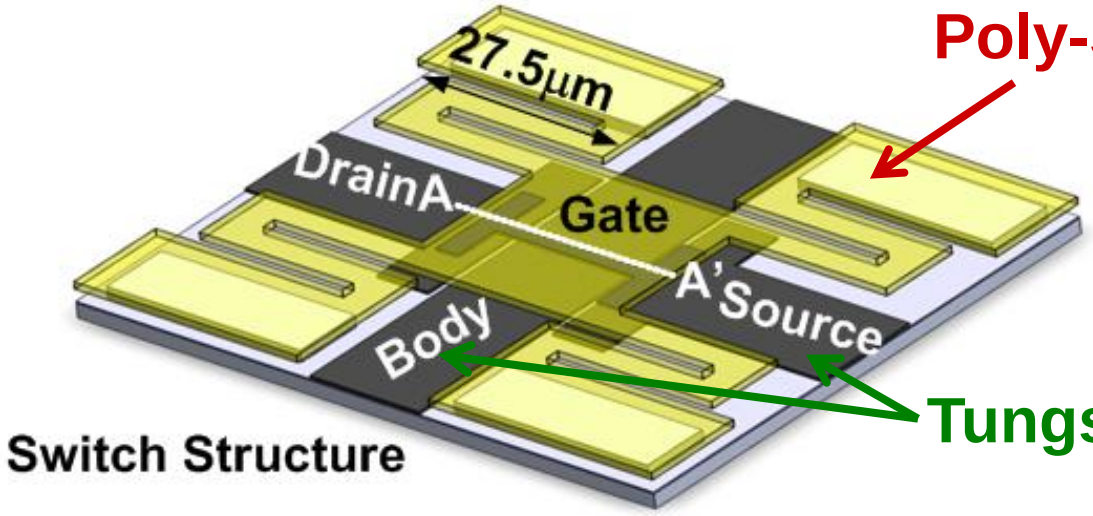
Measured MEM Relay IV*



- **Mechanical relays don't leak, turn on abruptly**
  - Potential pathway to continued energy scaling
- **Device/circuit co-design critical**

R. Nathanael *et al*., "4-Terminal Relay Technology for Complementary Logic," *IEDM 2009*

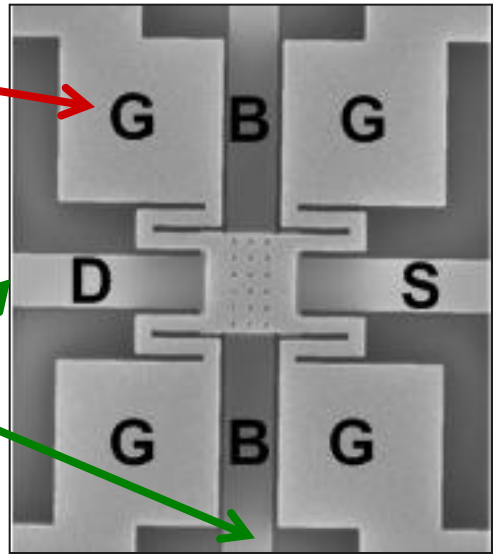
Relay Structure and Operation

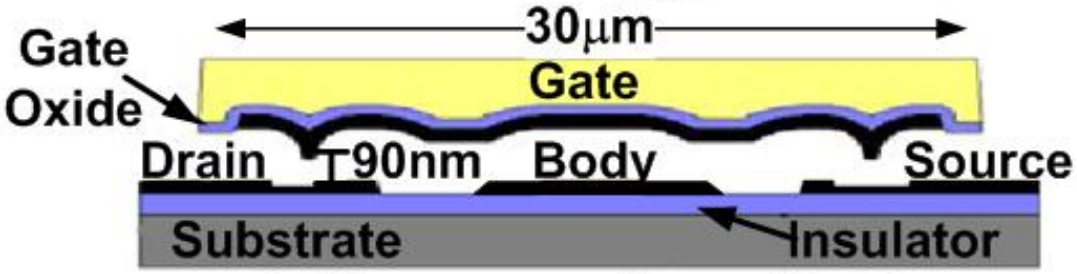


Switch Structure

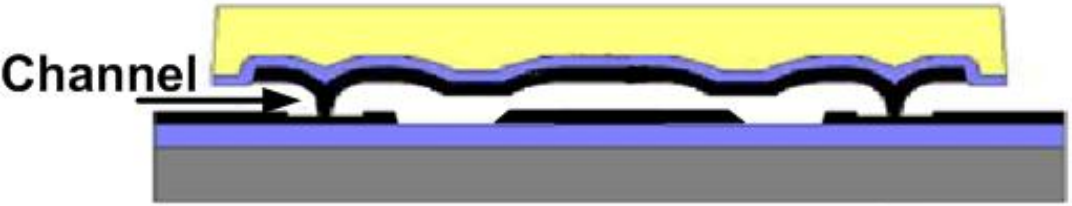
Poly-SiGe

Tungsten





A-A' cross-section: *off*-state



A-A' cross-section: *on*-state

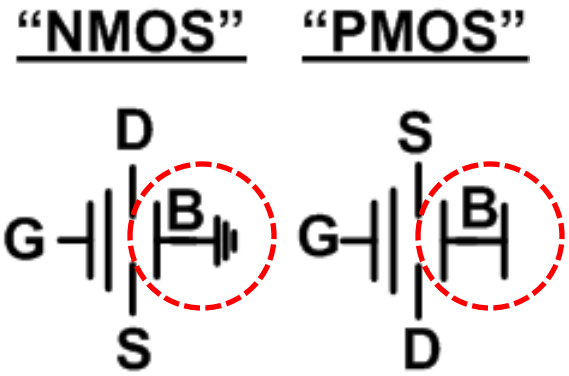
OFF:

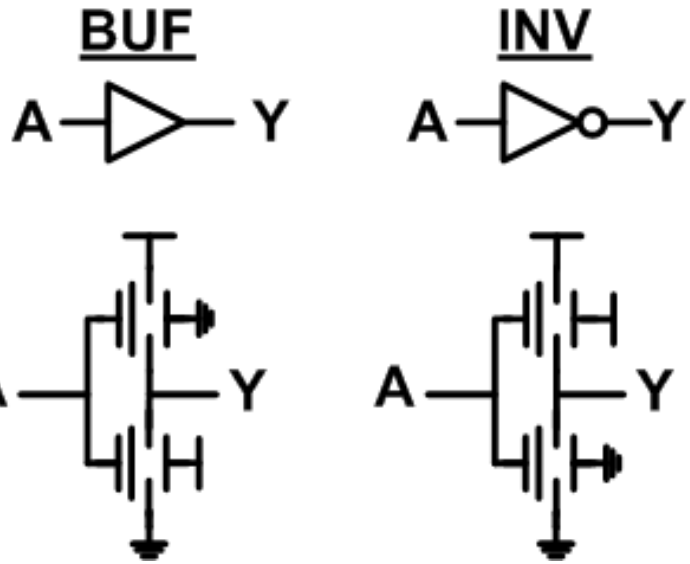
$|V_{gb}| < V_{po}$ (pull-out)

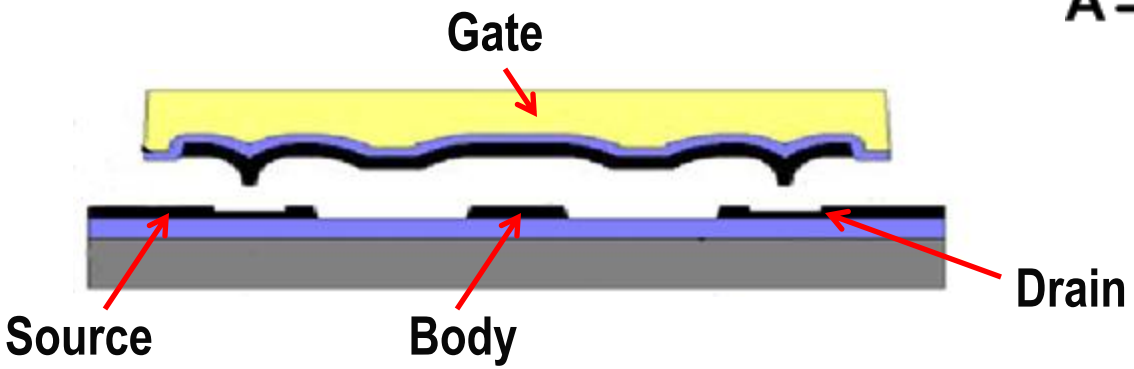
ON:

$|V_{gb}| > V_{pi}$ (pull-in)

NEM Relay as a Logic Element



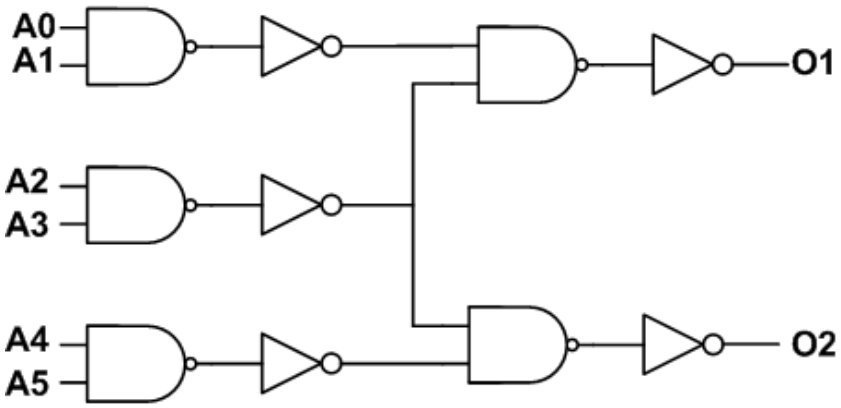




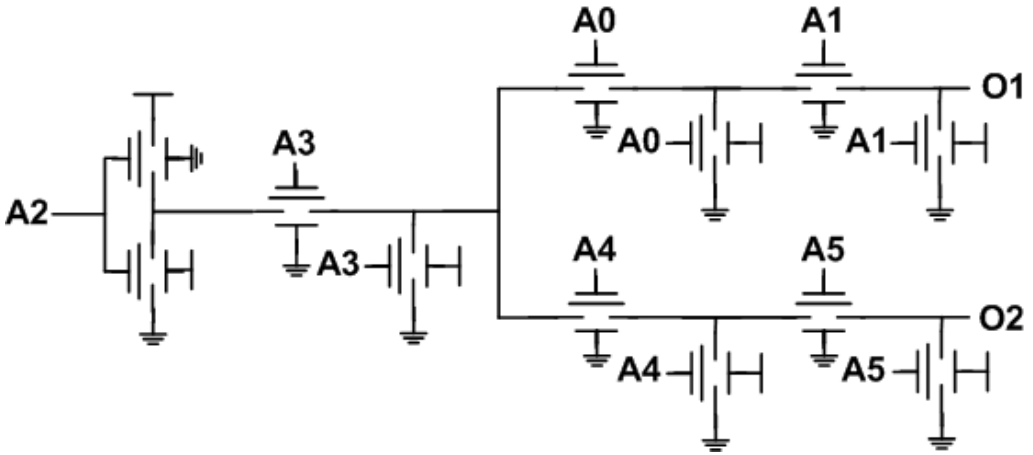
- **Mimics operation of CMOS transistors**
  - Electrostatic actuation is ambipolar
- **Unlike CMOS, non-inverting logic is possible**
  - Switch state set only by gate-to-body voltage

Digital Circuit Design with NEM Relays

CMOS: 30 transistors



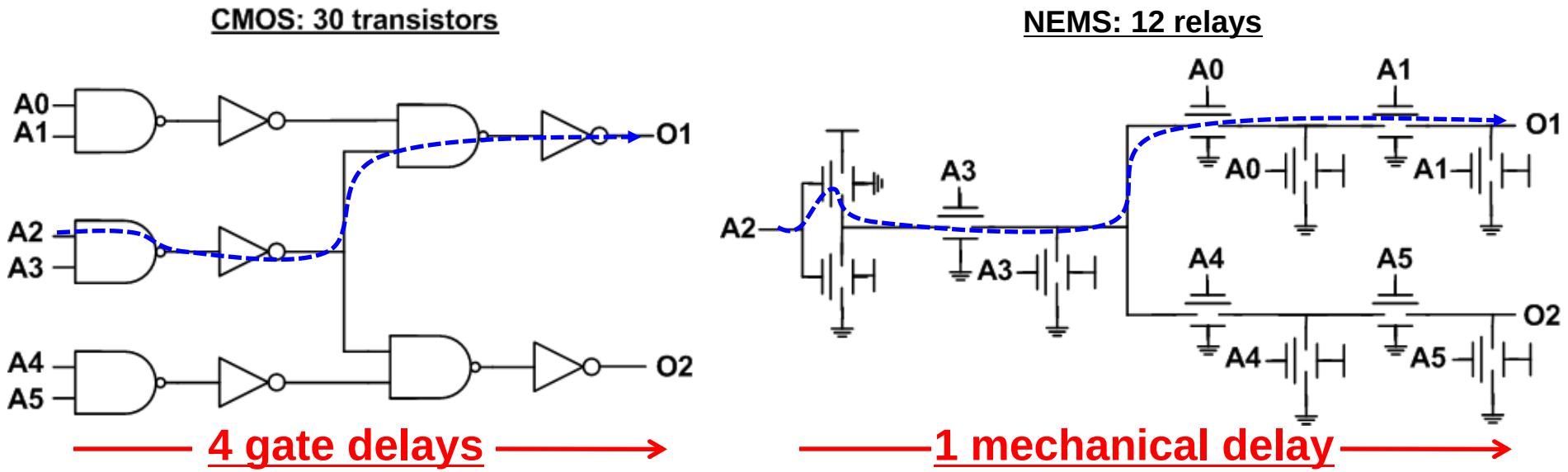
NEMS: 12 switches



- **CMOS: delay set by electrical time constant**
  - Cascade simple gates to distribute fanout
- **Relays: delay dominated by mechanical movement**
  - So, want all to switch simultaneously

→ **Implement logic as a single complex gate (1930's)**

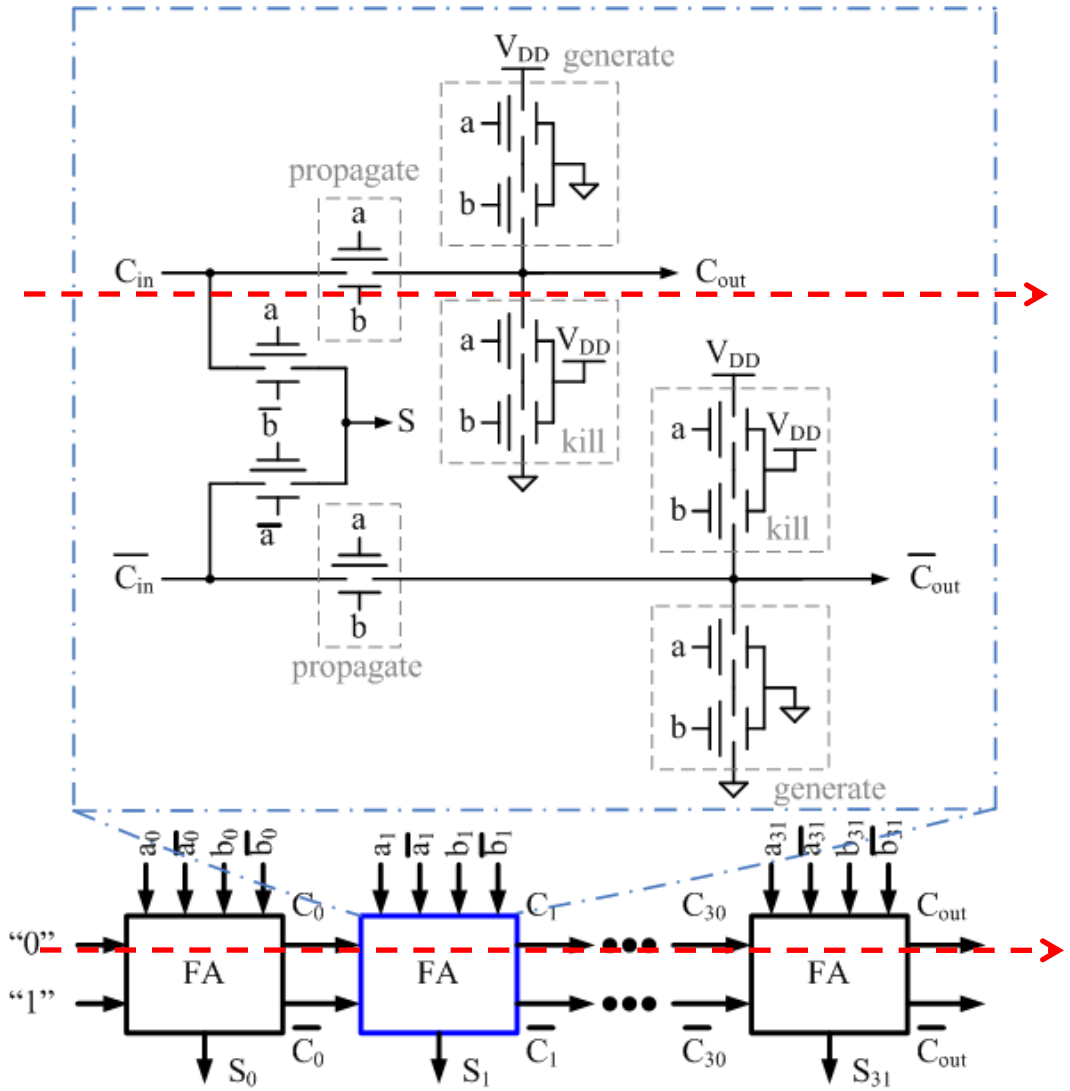
Need to Compare at Block Level



- **Single mechanical delay per block**
  - Substantially mitigates perceived delay disadvantage
- **Often fewer devices for same function**
  - Comparable area despite larger individual devices

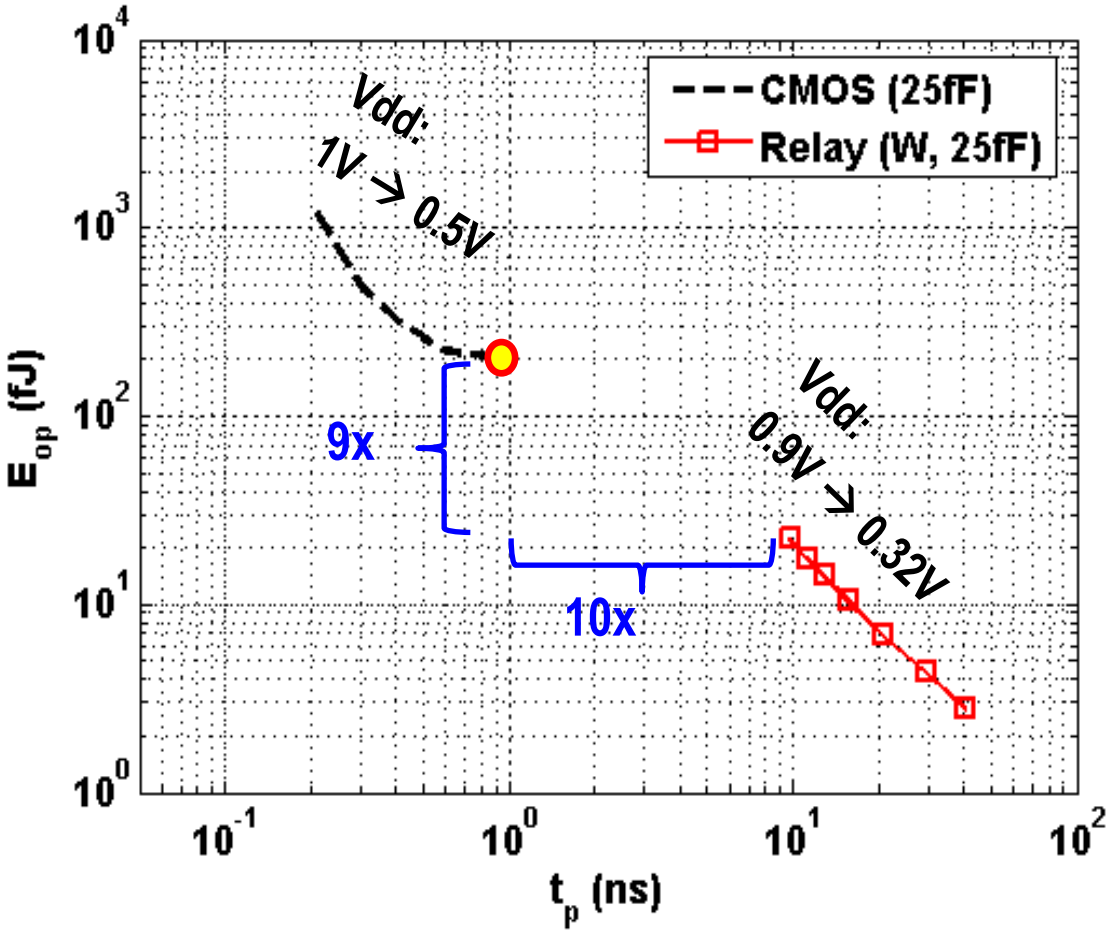
F. Chen *et al.*, "Integrated Circuit Design with NEM Relays," *ICCAD 2008*

Example: 32-bit Relay Adder



- **Ripple carry configuration**
  - Cascade full adder cells to create larger complex gate
- **Stack of 32 relays, still a single mechanical delay**

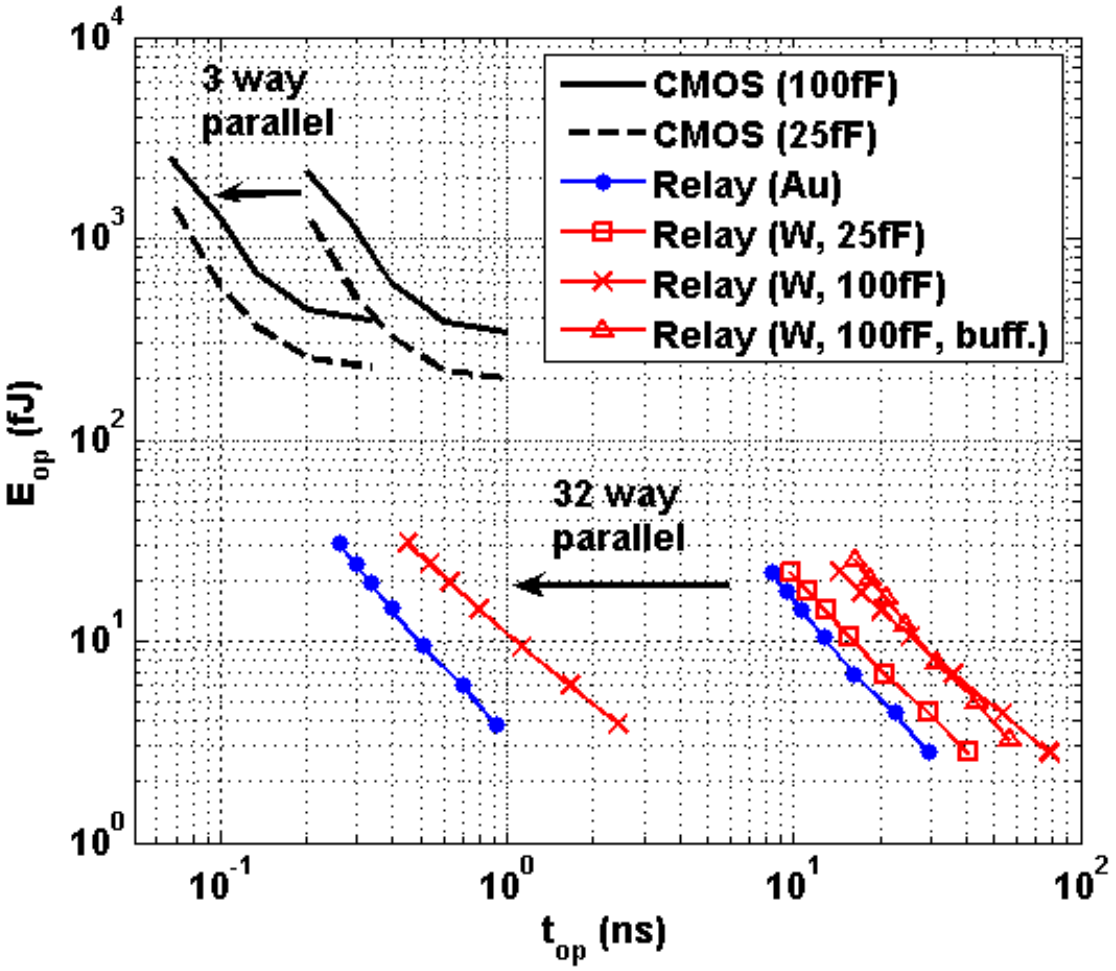
Scaled Relay vs. CMOS Adders



- **Compare vs. CMOS adder* in 90nm technology**
- **For similar area:**
  >9x lower E/op
  >10x greater delay

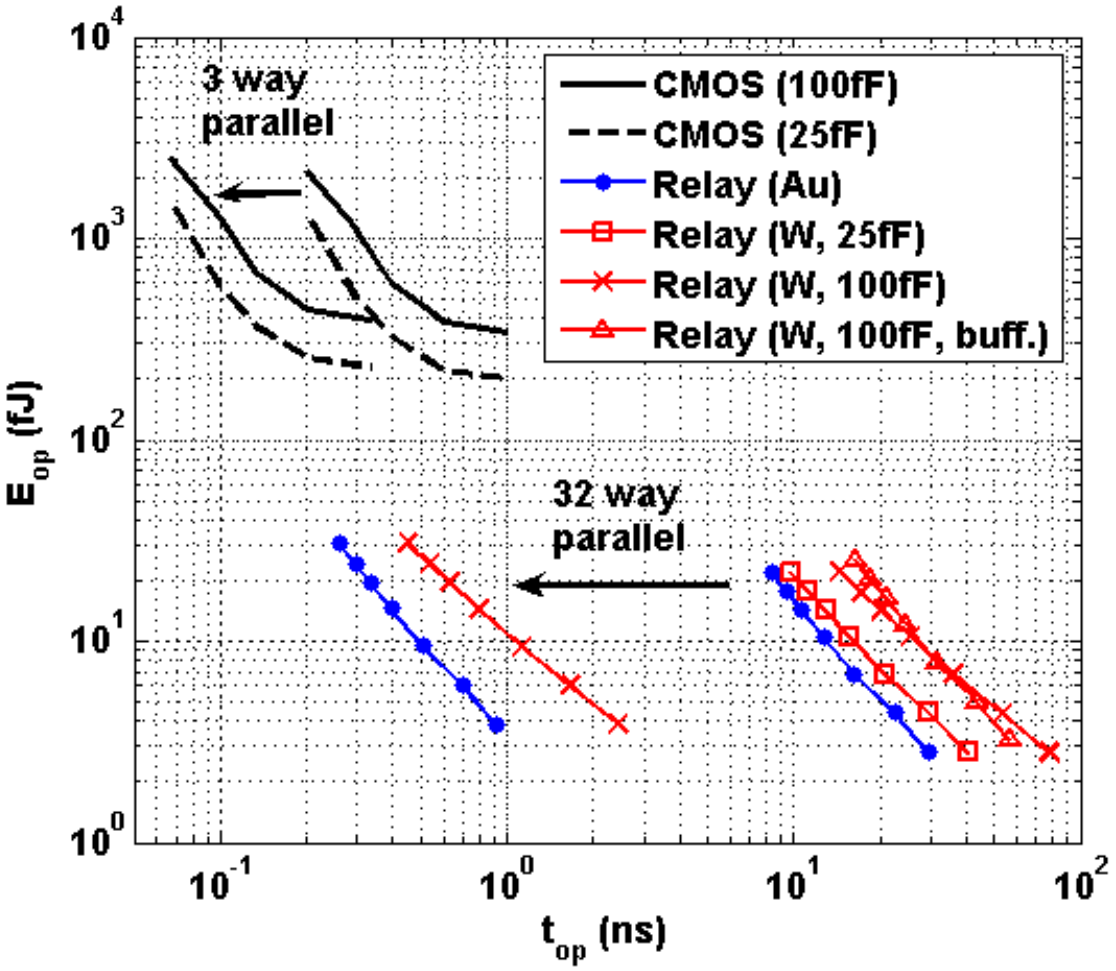
* D. Patil *et al.*, "Robust Energy-Efficient Adder Topologies," *ARITH 2007*

Parallelism



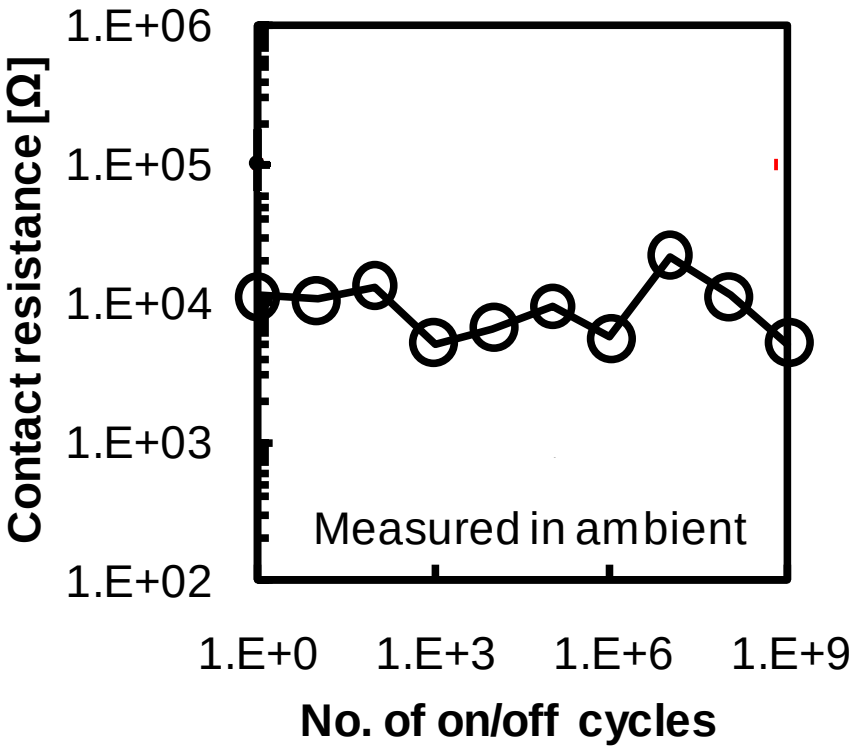
- **Can extend energy benefit up to GOPS throughput**
  - As long as parallelism is available

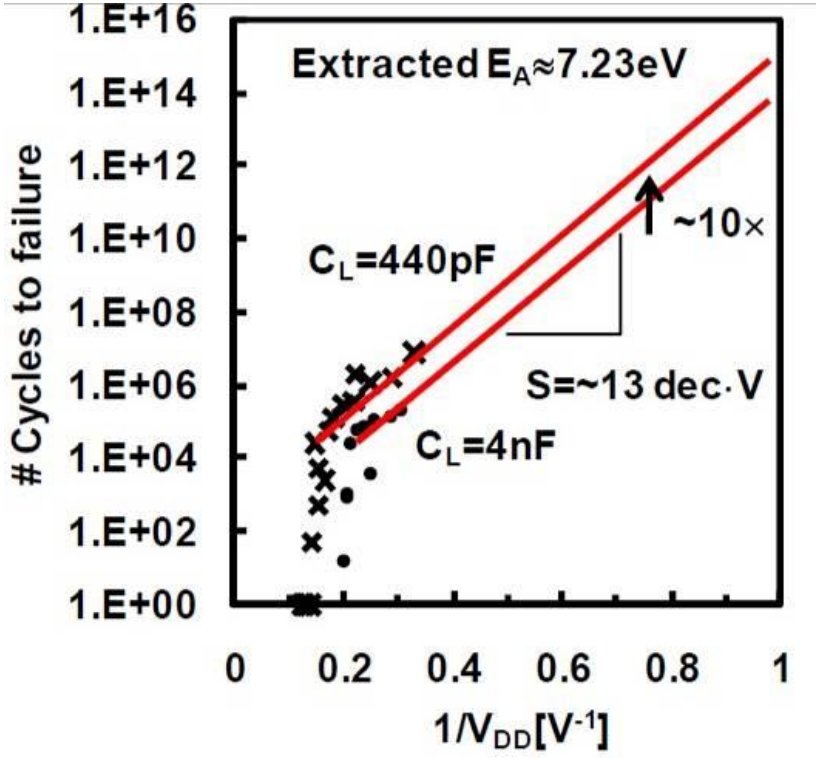
Contact Resistance



- Low contact R not critical
- Good news for reliability…

Relay Contact Reliability



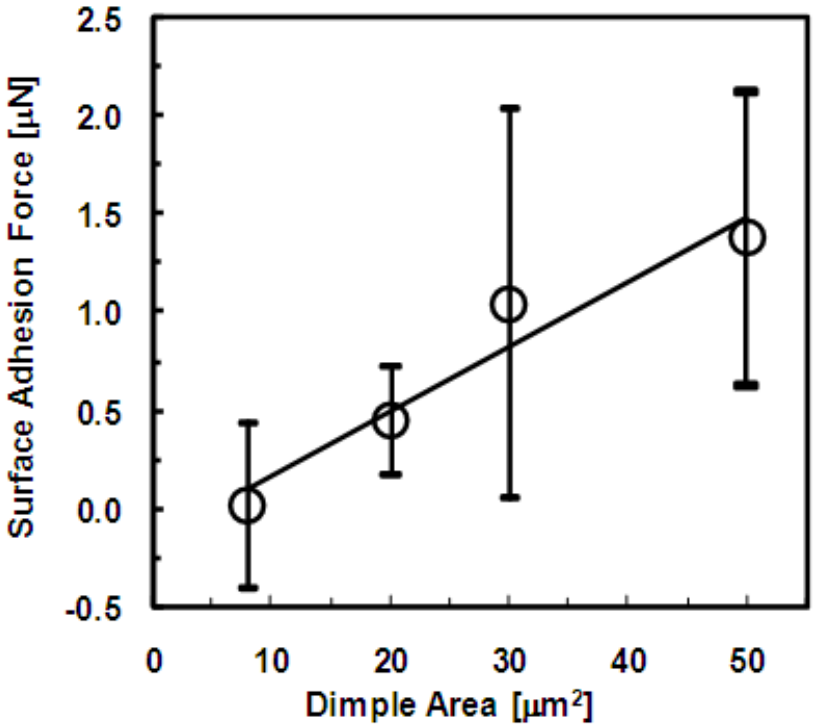


- **Higher contact R, hard contact (W) improves reliability**
  - Limits power dissipation, material flow
- **Current endurance record: 65 billion cycles**
  - Theory/experiments predict >10^{15} cycles @ 1V VDD

H. Kam *et al.*, *IEDM 2010*

Relay Energy Limit

- **Spring force must be able to overcome surface adhesion force F_A:**
  - $E_{min} = 2F_A g_d \approx 2E_{surf}$
- **For large contacts, F_A scales with area**



- **Extracted surface adhesion energy ~5μJ/m²**
  - 90nm x 90nm: E_{surf} = .04aJ!
- **Ultimate energy limit set by # of contact bonds**
  - ~0.2aJ per bond

H. Kam *et al.*, *IEDM 2009*

Conclusions

- **Relay characteristics enable energy scaling beyond CMOS**
  - Nearly ideal I_{on}/I_{off}
  - Need to adapt circuit design style
- **Reliability improving**
  - Circuit level insights critical (contact R)
- **Potential for 10X or more lower E/op than CMOS**
  - How to build complex relay-based systems?
  - Will this really work in practice?