Discrete-Time, Cyclostationary Phase-Locked Loop Model for Jitter Analysis

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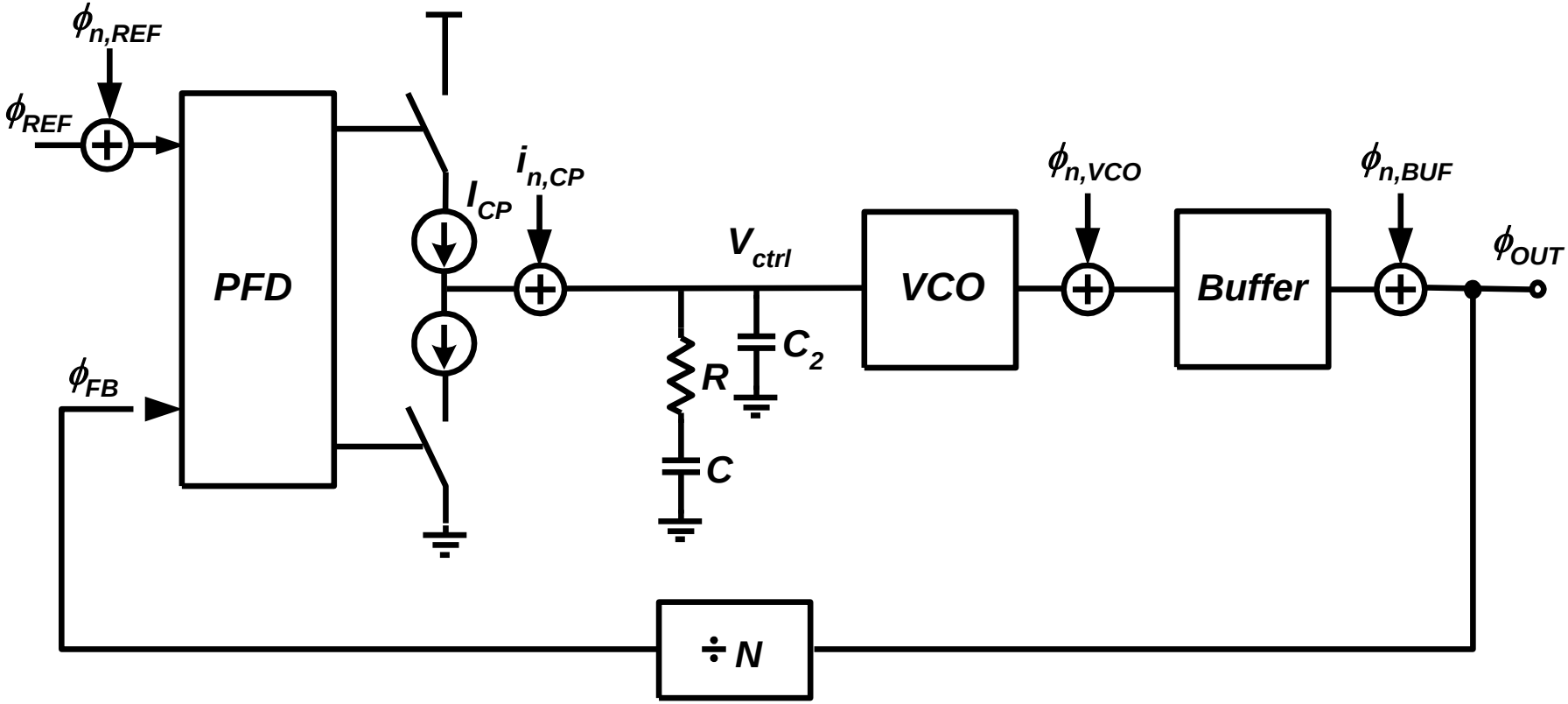
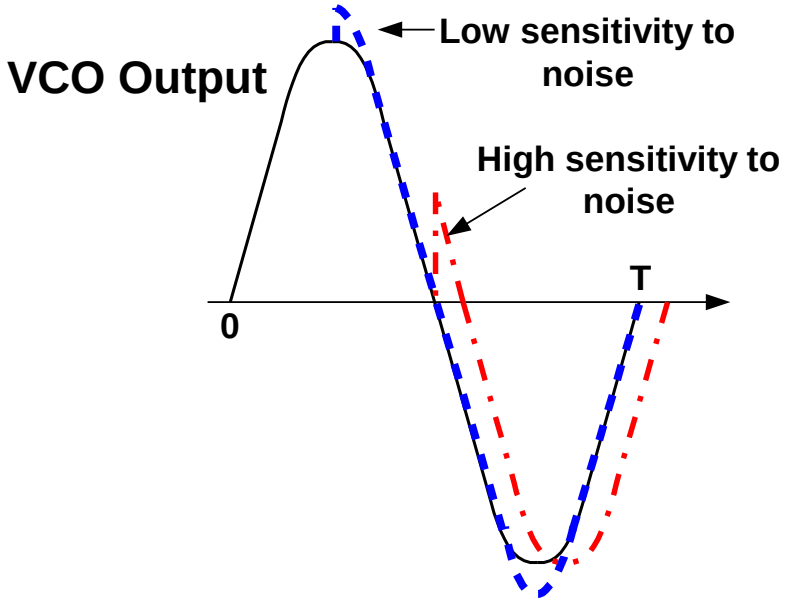
Problem Statement



- **Conventional approach for PLL jitter analysis:**
  - PLL is modeled as continuous-time, linear, time-invariant system (s-domain)
  - Problem: None of these assumptions are really accurate

Problem Statement

- Issues:
  - Time invariance assumption:
  - In reality: Noise effect on jitter is cyclostationary
  - *Time-invariant analysis cannot capture this effect*



  - Continuous-time assumption:
  - In reality:
    - Jitter is a discrete-time signal.
    - Jitter aliasing may occur when PLL divide ratio different than 1.
  - *Continuous-time analysis cannot capture this effect*

Previous Approaches

- **Discrete-time analysis:**
  - Divide ratio N=1 [1,2] or
  - Divide-by-N block is modeled as 1/N [3]
- **Cyclostationary analysis [4]:**
  - Circuit-specific
  - Limited to VCO supply/substrate noise

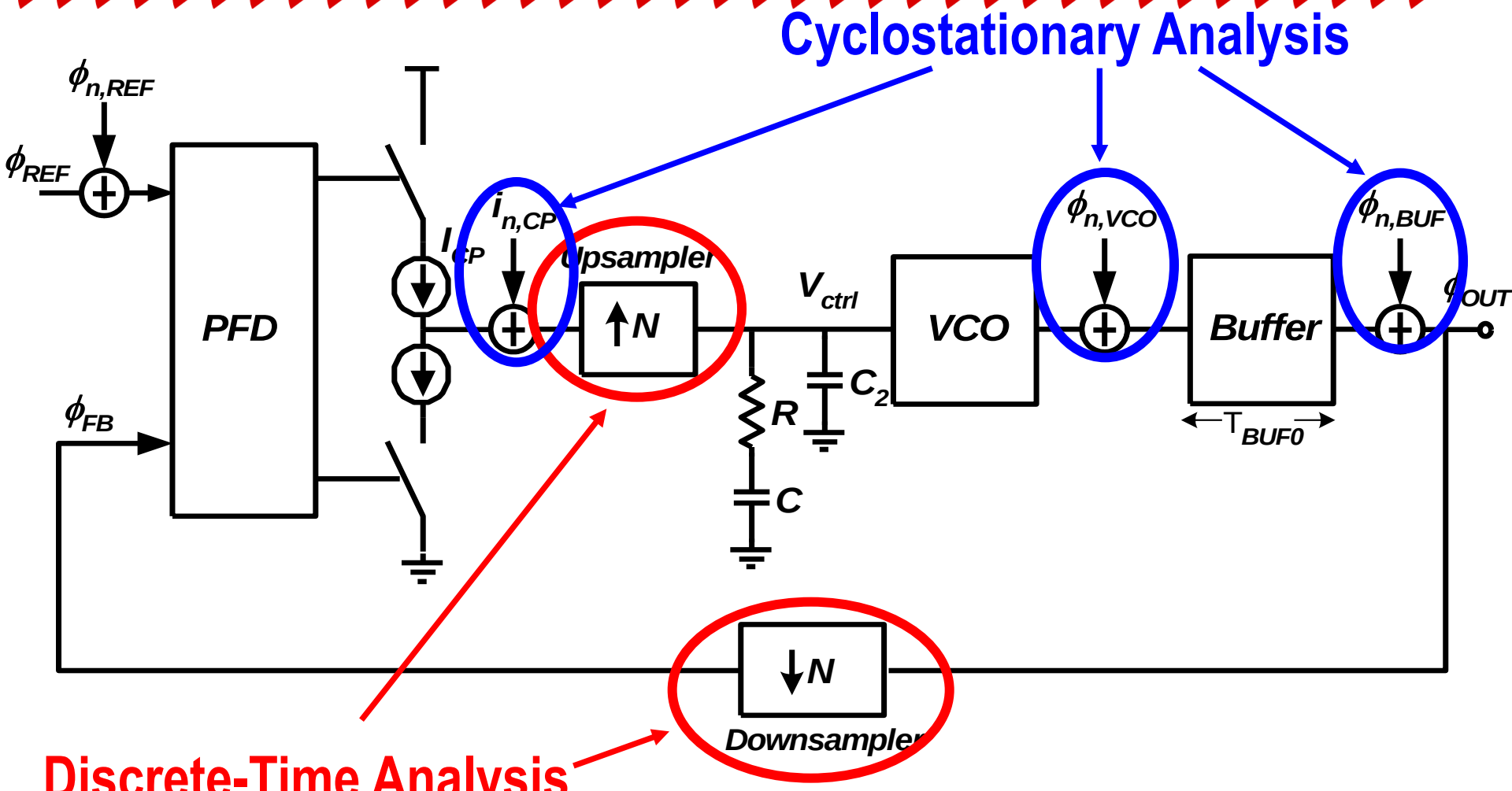
[1] J. P. Hein and J. W. Scott, 1988.

[2] P. K. Hanumolu, M. Brownlee et al., 2004.

[3] J. Lu, B. Grung et al., 2001.

[4] P. Heydari, 2004.

Discrete-Time, Cyclostationary PLL Model



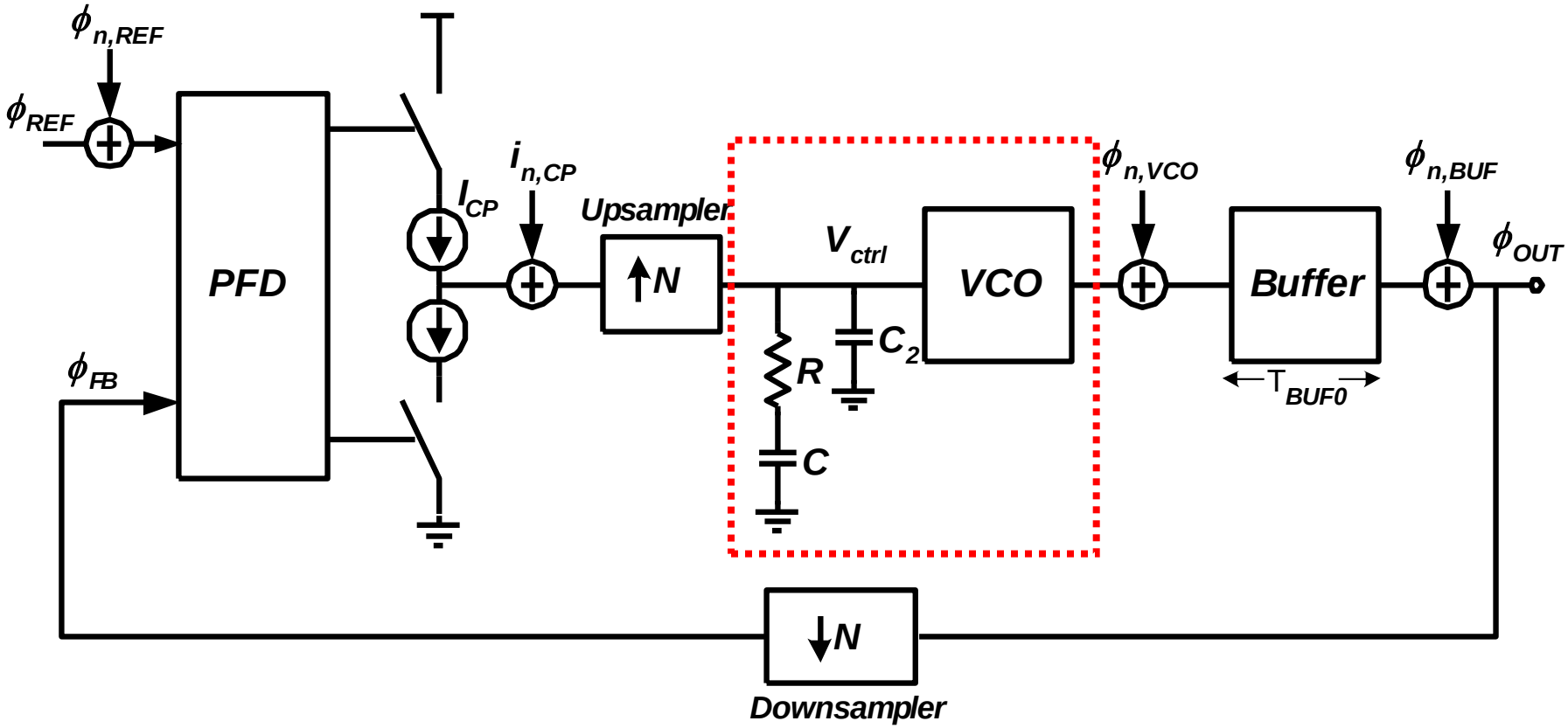
Upsampler-by-N: Charge pump produces current pulses once every N PLL periods.

Development of PLL Model

Steps:

- **Discrete-time description of PLL components**
  - **Loop filter, VCO, divide-by-N**
- **Calculation of noise spectra injected into PLL loop**
  - **Take into account cyclostationary noise behavior**
- **Calculation of discrete-time PLL dynamics**

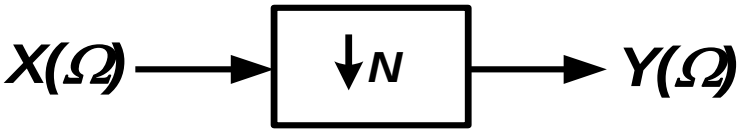
PLL Components in Discrete-Time

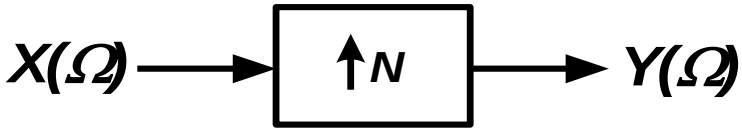


Combination of Loop Filter & VCO modeled through impulse-invariant transformation.

J. P. Hein and J. W. Scott, 1988.

PLL Components in Discrete-Time





$$Y(\Omega) = \frac{1}{N} \cdot \sum_{k=0}^{N-1} X\left(\frac{\Omega - 2\pi k}{N}\right)$$

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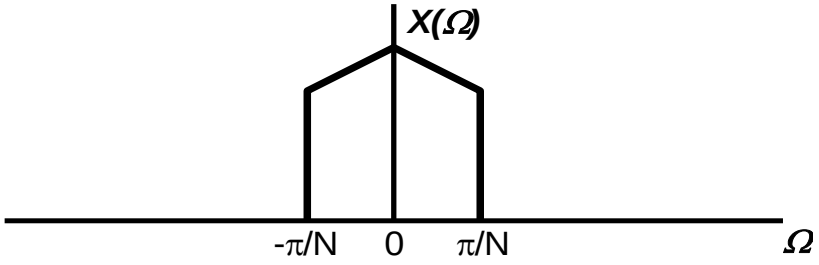
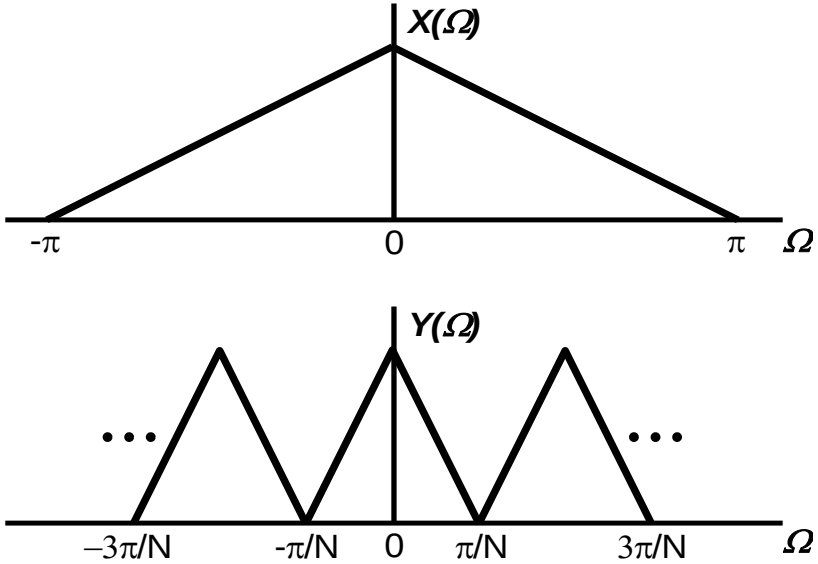
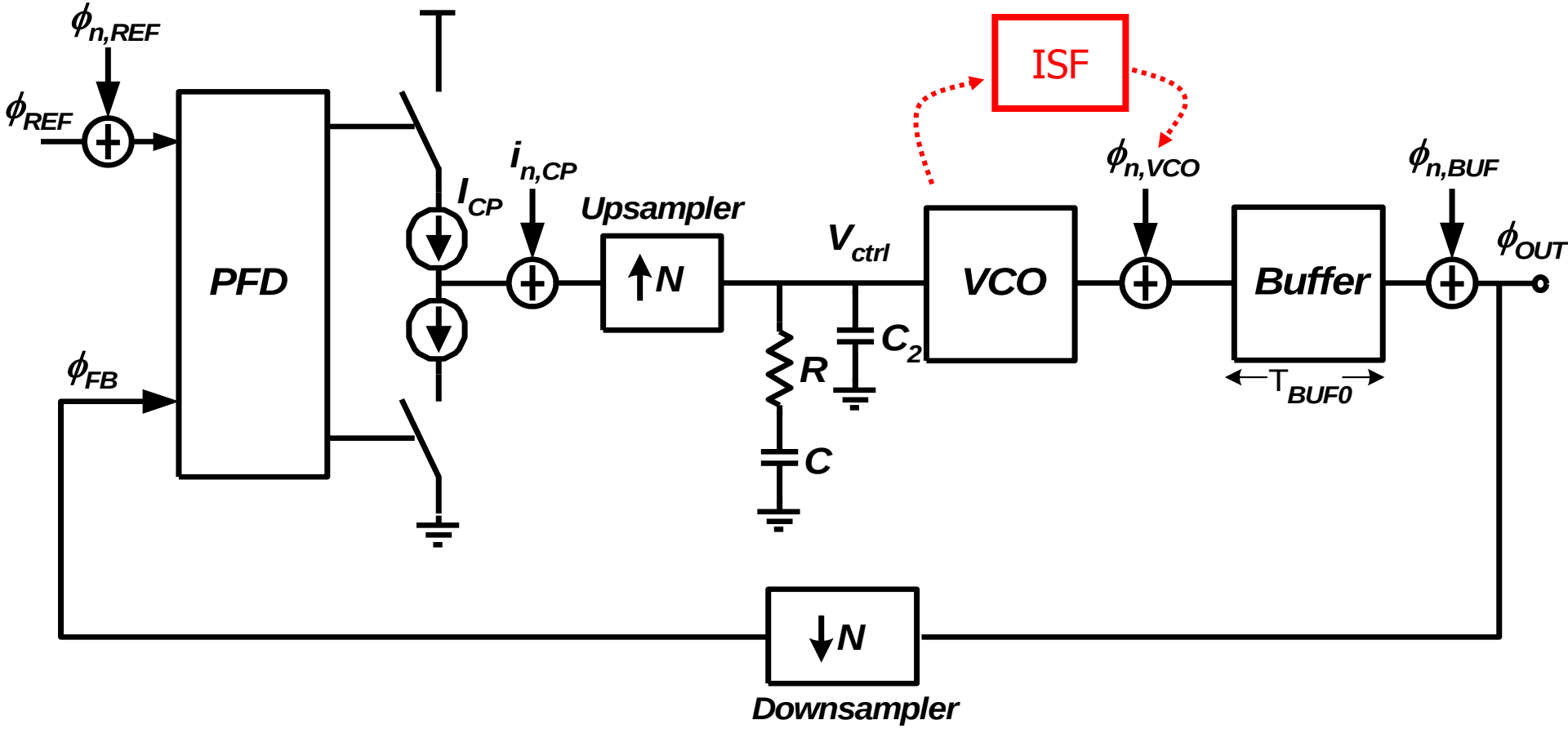




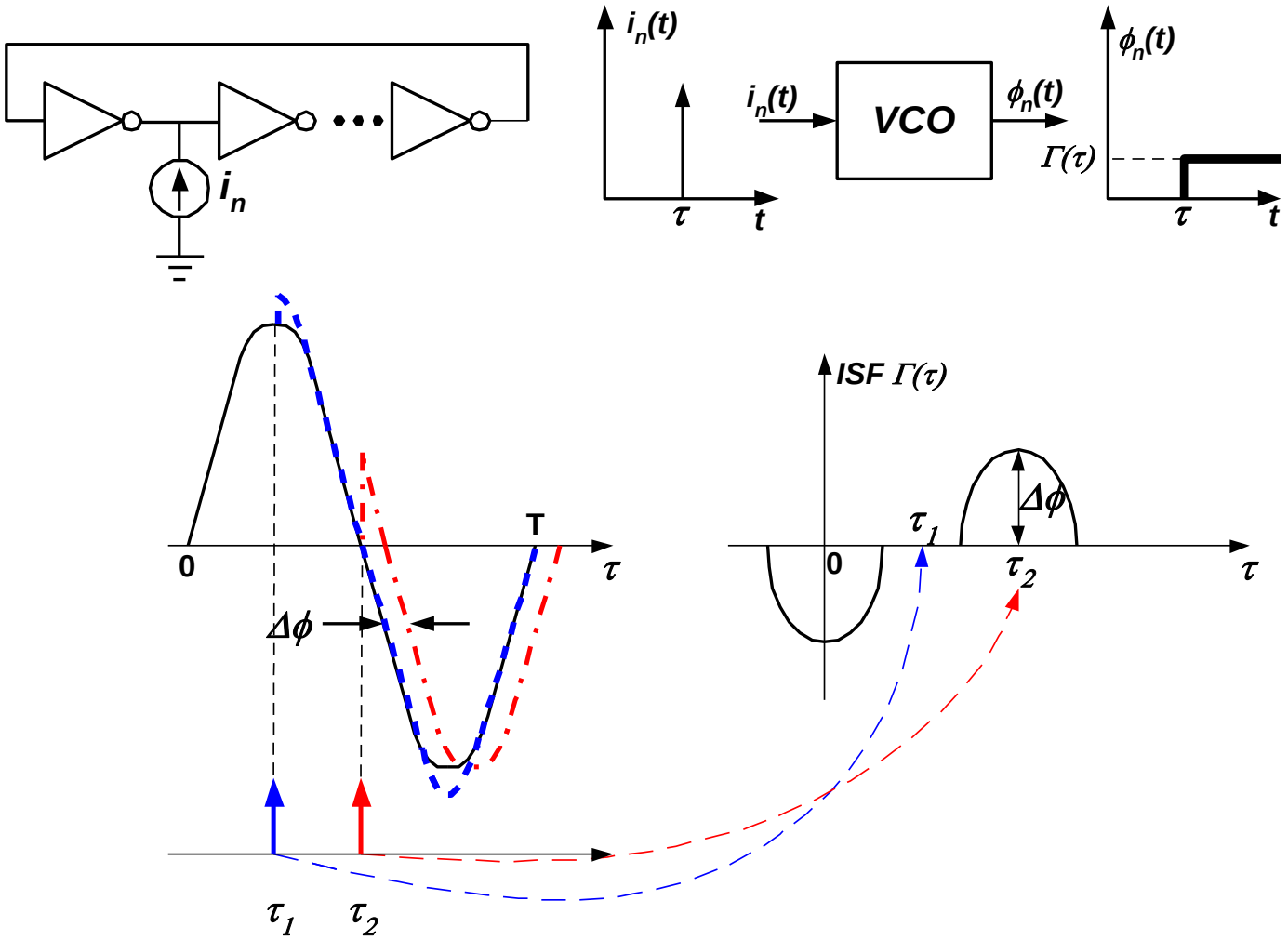
Injected PLL Loop Noise



Noise injected into PLL loop is modulated by Impulse Sensitivity Function (ISF).

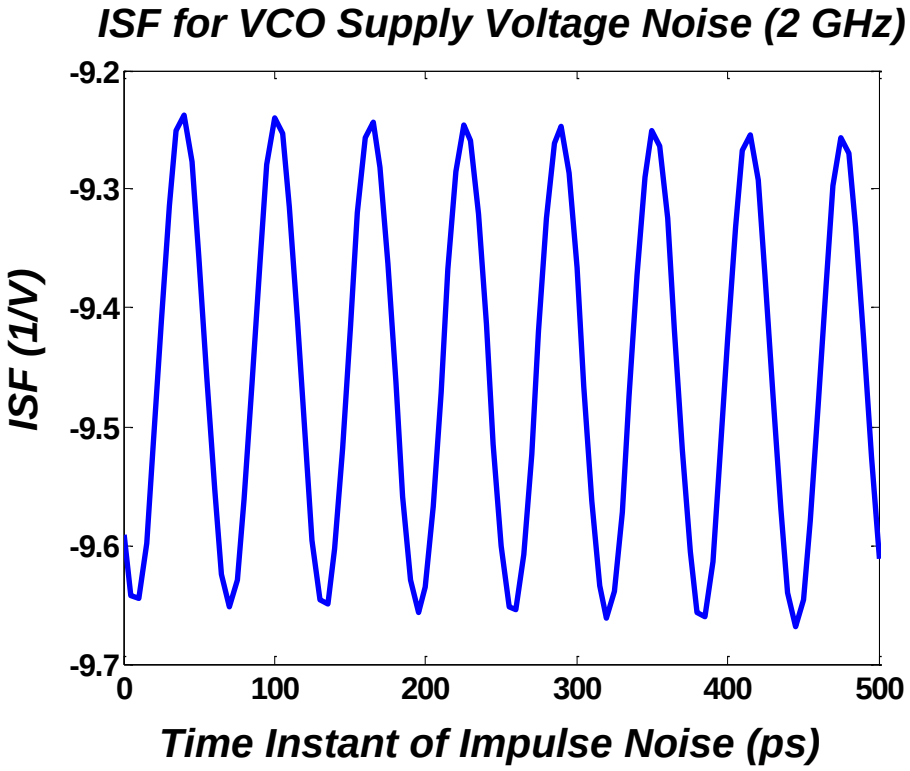
A. Hajimiri and T. H. Lee, 1998.

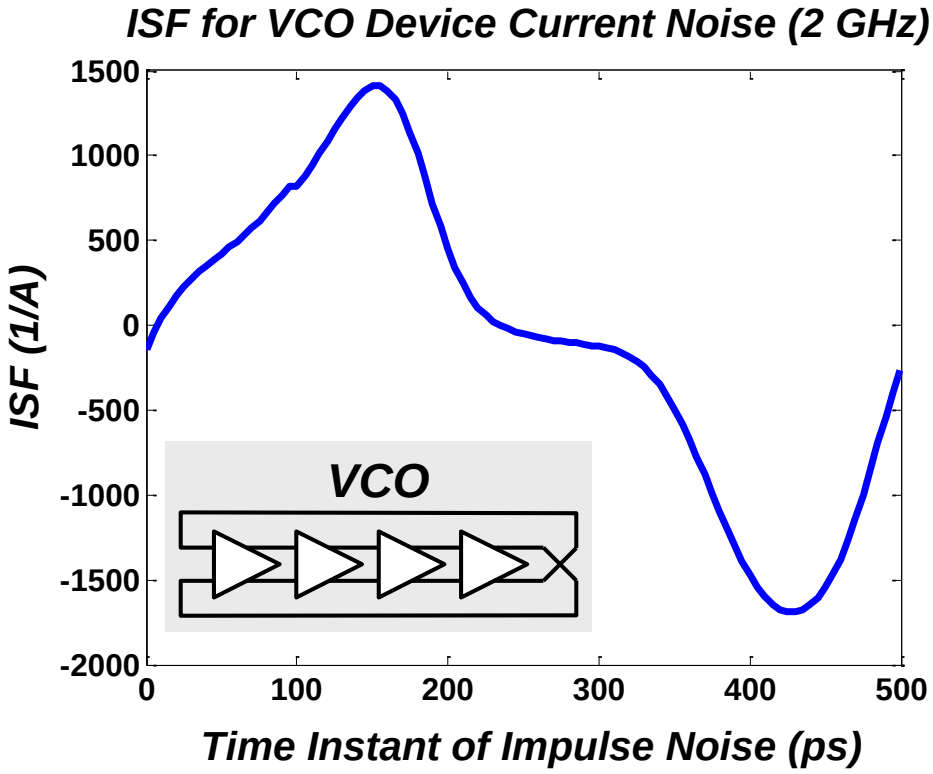
ISF Mechanism - VCO



- VCO phase impulse response is step function.
- Analysis valid for both supply/substrate and device noise.

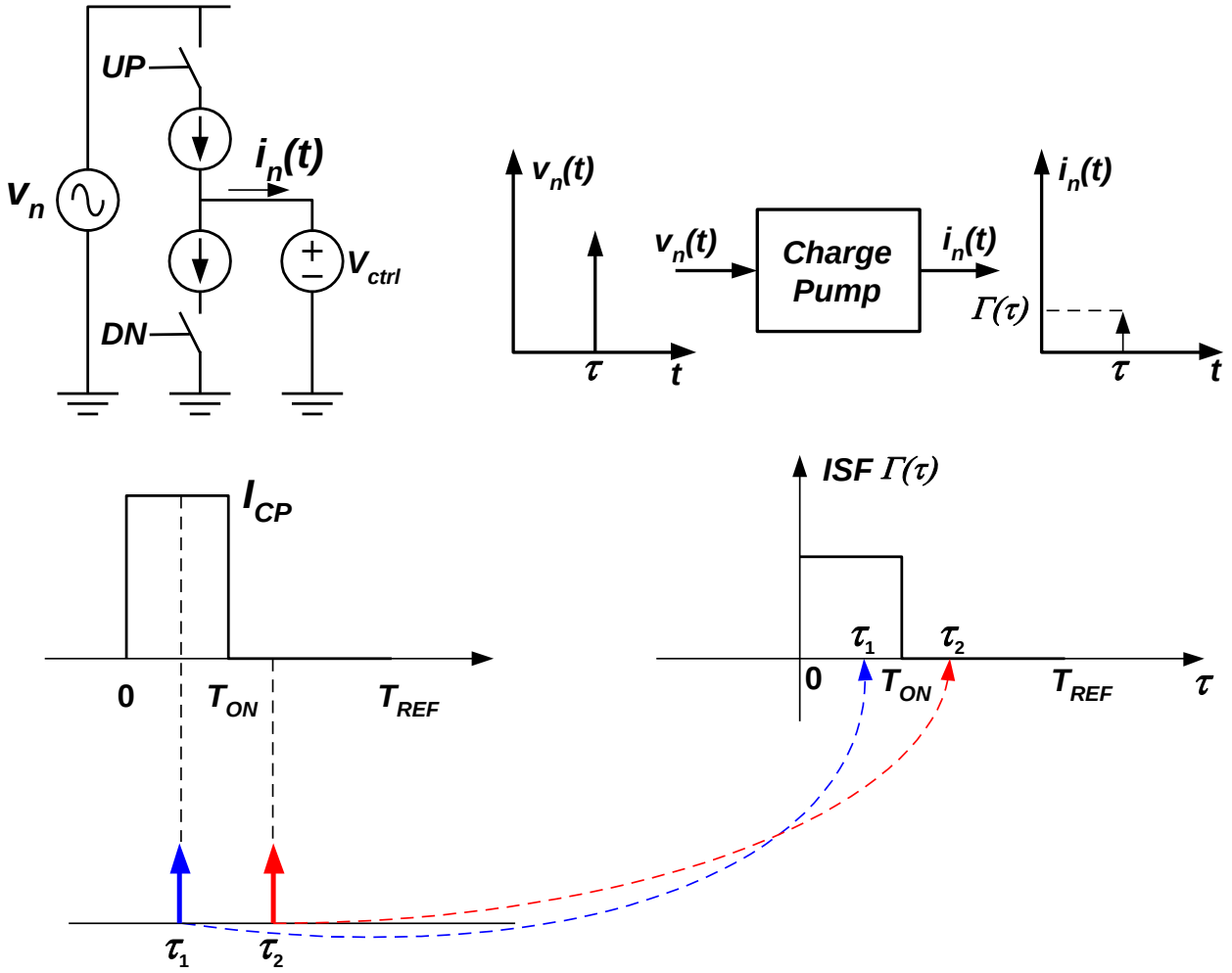
ISF Mechanism - VCO





ISFs obtained for VCO with 4 differential stages @ 2 GHz.

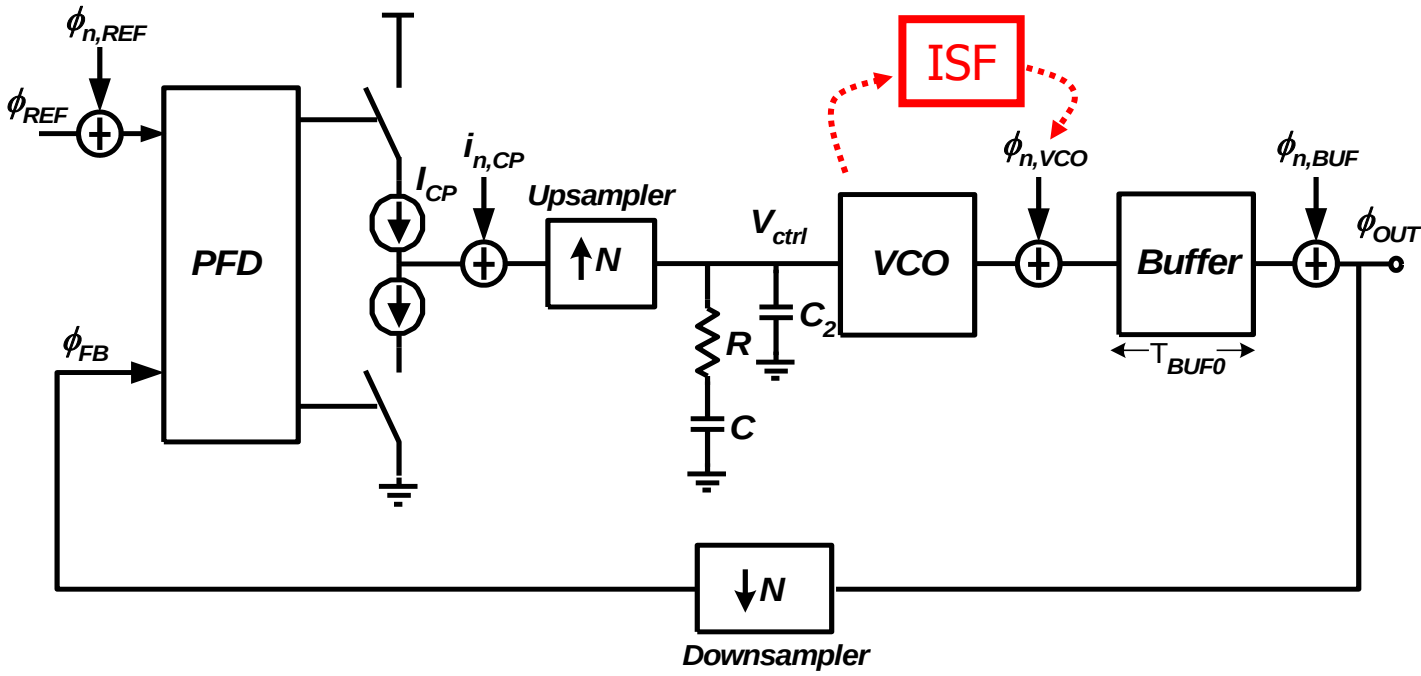
ISF Mechanism – Charge Pump



- Charge pump current impulse response is impulse function.
- Charge pump ISF is non-zero and almost constant during T_{ON}.

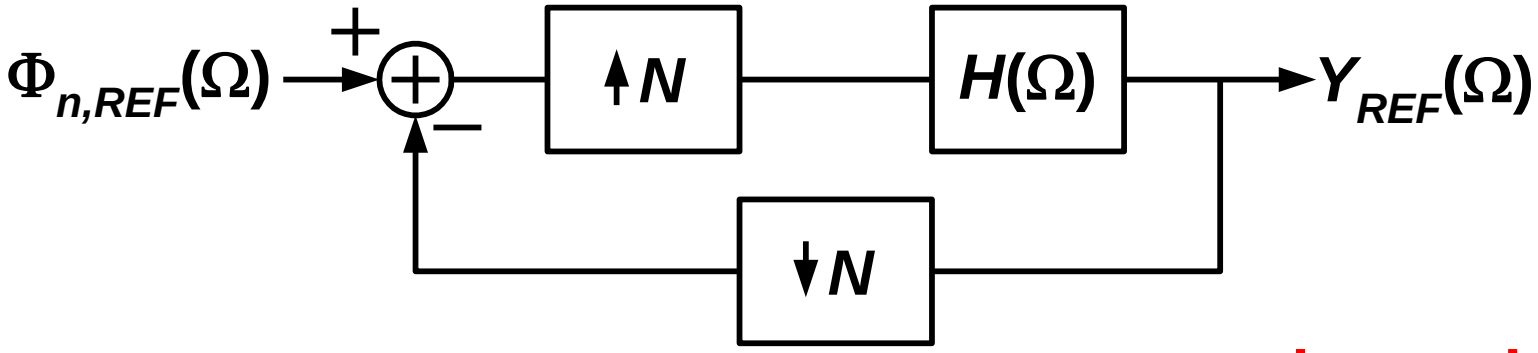
Injected PLL Loop Noise

- **Calculate injected PLL loop noise at the output of PLL components (VCO, charge pump, VCO buffer) by filtering the supply/device noise through the ISF.**
- **Cases of supply/device noise:**
  - Impulse
  - Step
  - White
  - Sinusoidal



Discrete-Time PLL Dynamics

RefClk Noise (H is the forward transfer function of the PLL):



Jitter Spectrum:

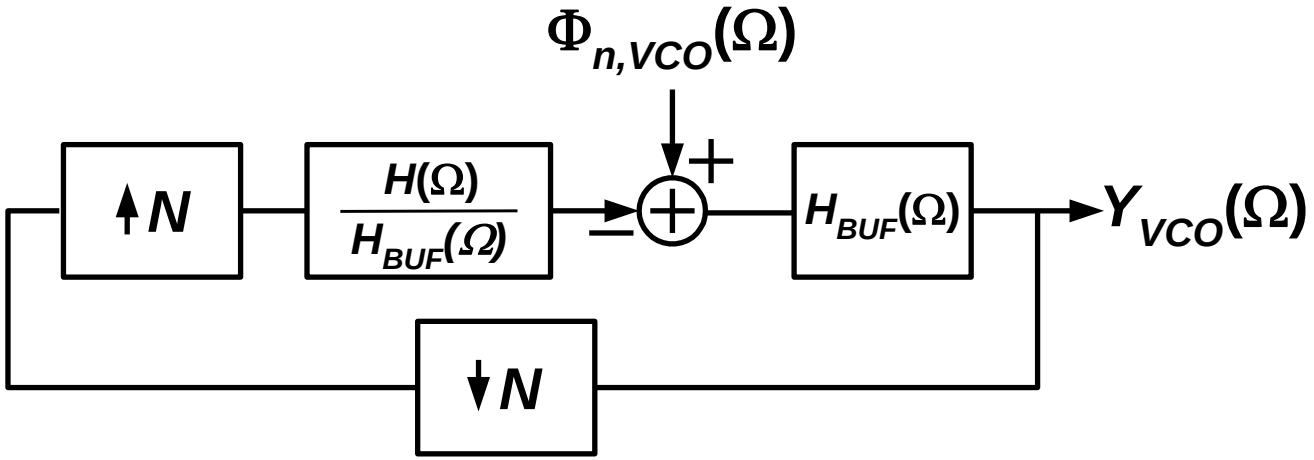
$$Y_{REF}(\Omega) = \frac{H(\Omega)}{1 + \frac{1}{N}\sum_{k=0}^{N-1} H\left(\Omega - \frac{2\pi k}{N}\right)} \cdot \Phi_{n,REF}(N \cdot \Omega)$$

Images!

Similar expression for charge pump.

Discrete-Time PLL Dynamics

Closed-Loop PLL Transfer Function for VCO Noise:



Aliasing!

Jitter Spectrum:

$$Y_{VCO}(\Omega) = \Phi_{n,VCO}(\Omega) - \frac{\frac{1}{N}\sum_{k=0}^{N-1}\Phi_{n,VCO}\left(\Omega - \frac{2\pi k}{N}\right)}{1+\frac{1}{N}\sum_{k=0}^{N-1}H\left(\Omega - \frac{2\pi k}{N}\right)} \times H(\Omega)$$

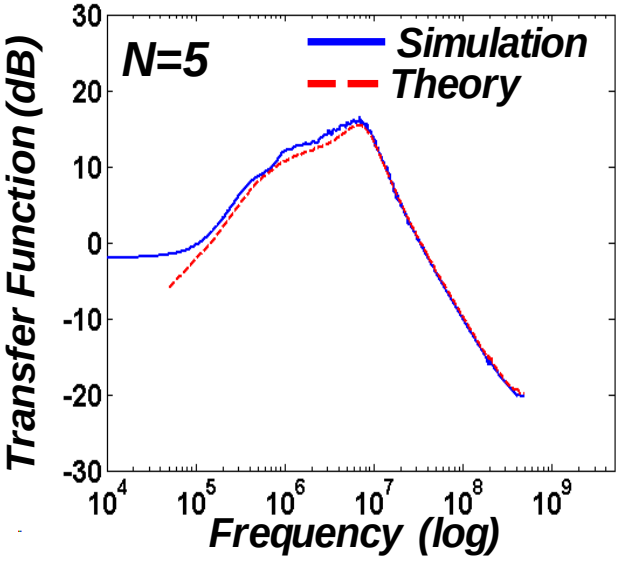
Similar expression for VCO buffer.

Theory vs. Simulation - Cyclostationarity

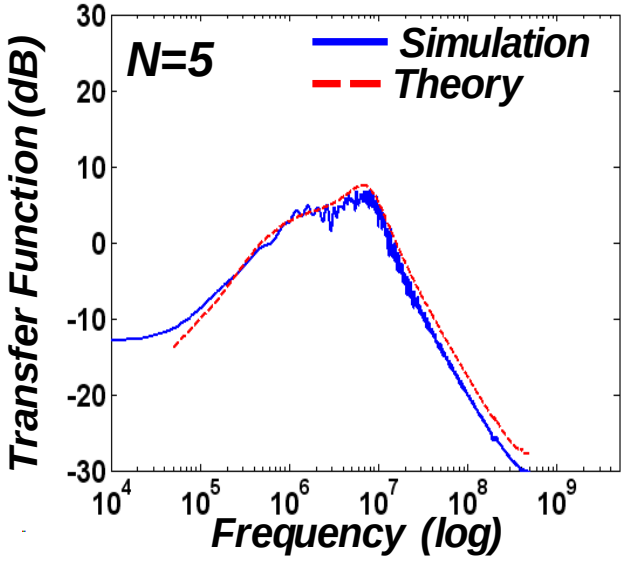
Simulation: 3rd-order PLL implemented in Verilog-A

VCO Impulse Noise applied at two different instants:
Magnitude of noise transfer function is different.

Transfer Functions from VCO Supply Noise to PLL Output Jitter



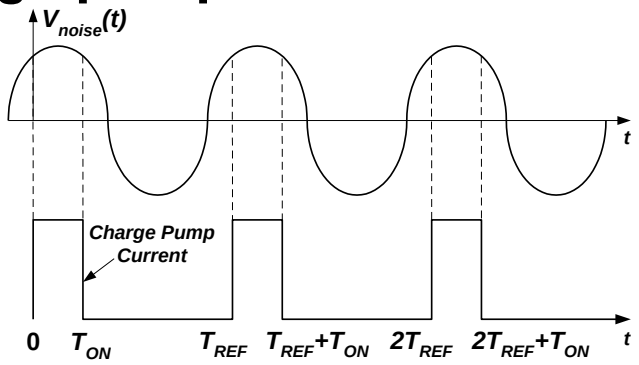
Impulse at max. VCO sensitivity

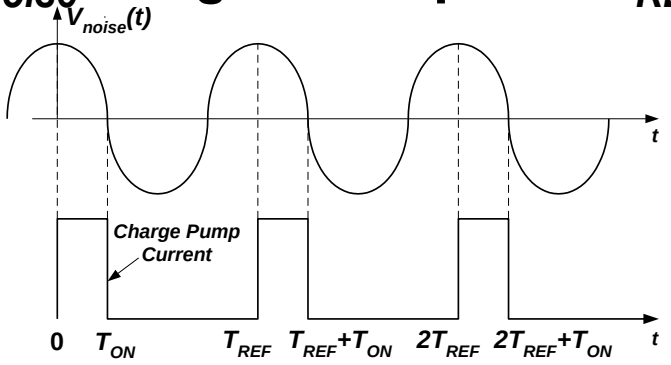


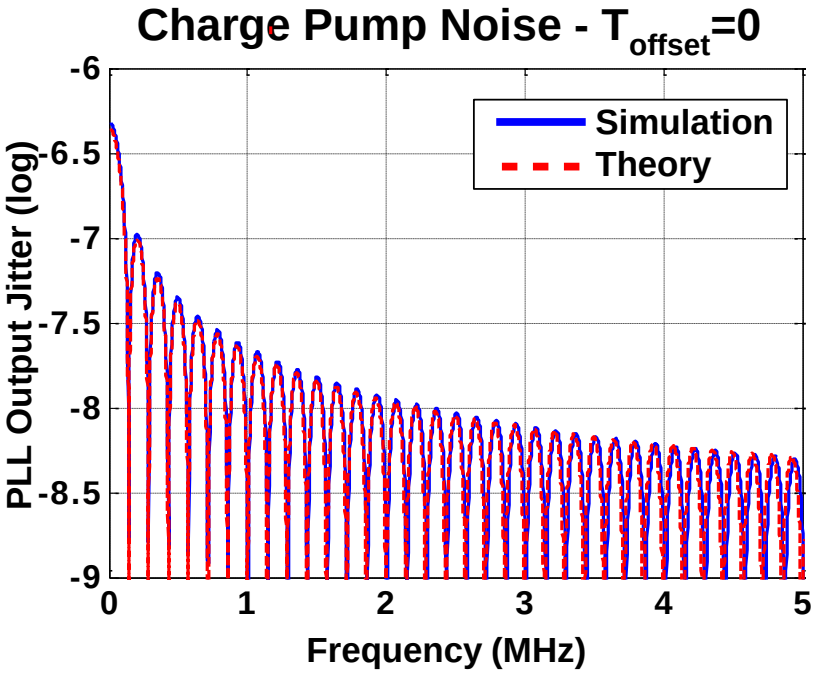
Impulse at 40% VCO sensitivity

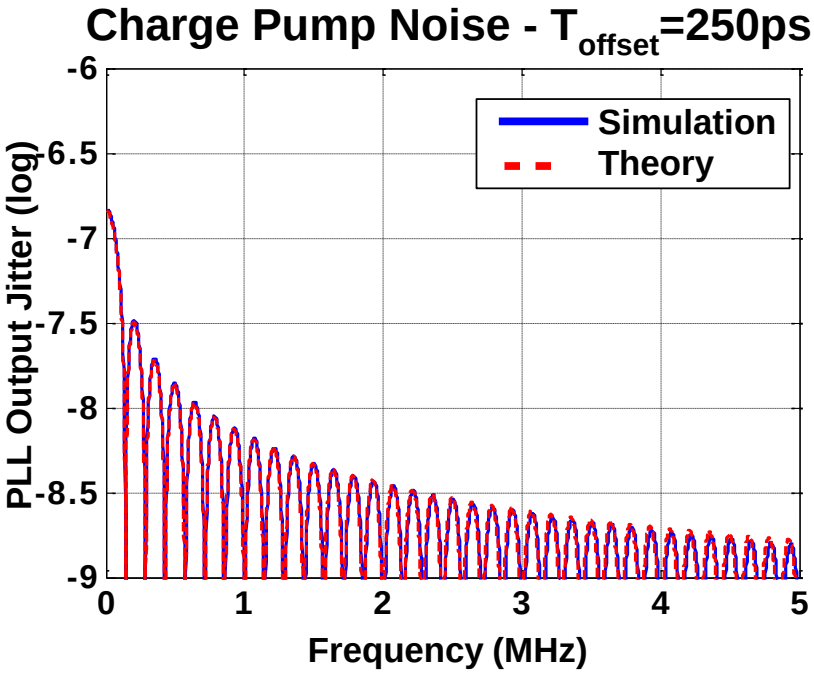
Theory vs. Simulation - Cyclostationarity

Charge pump sinusoidal noise with F_{noise} integer multiple of F_{REF}:





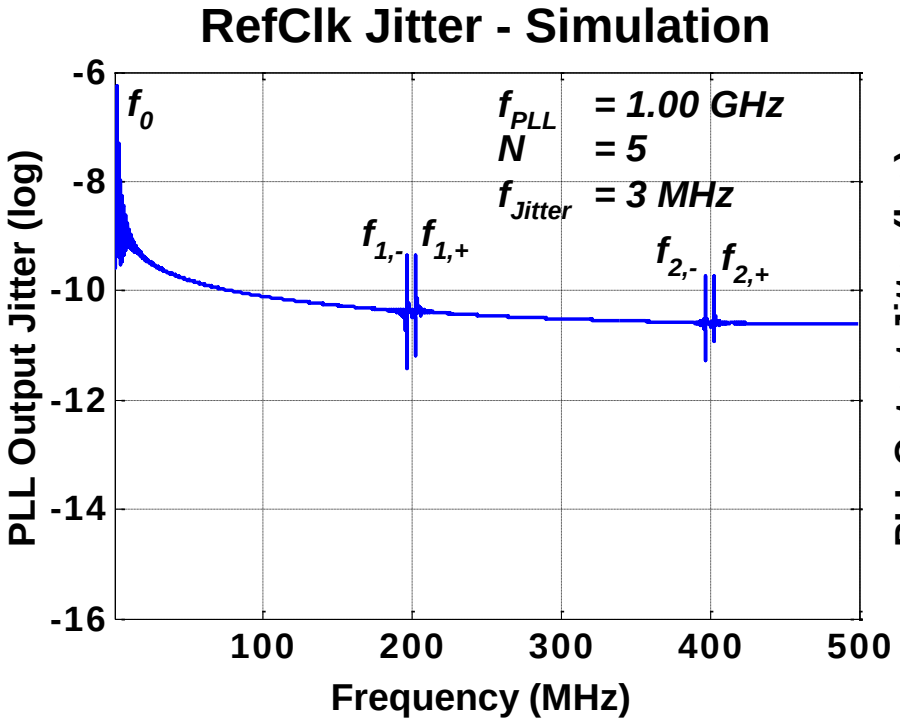


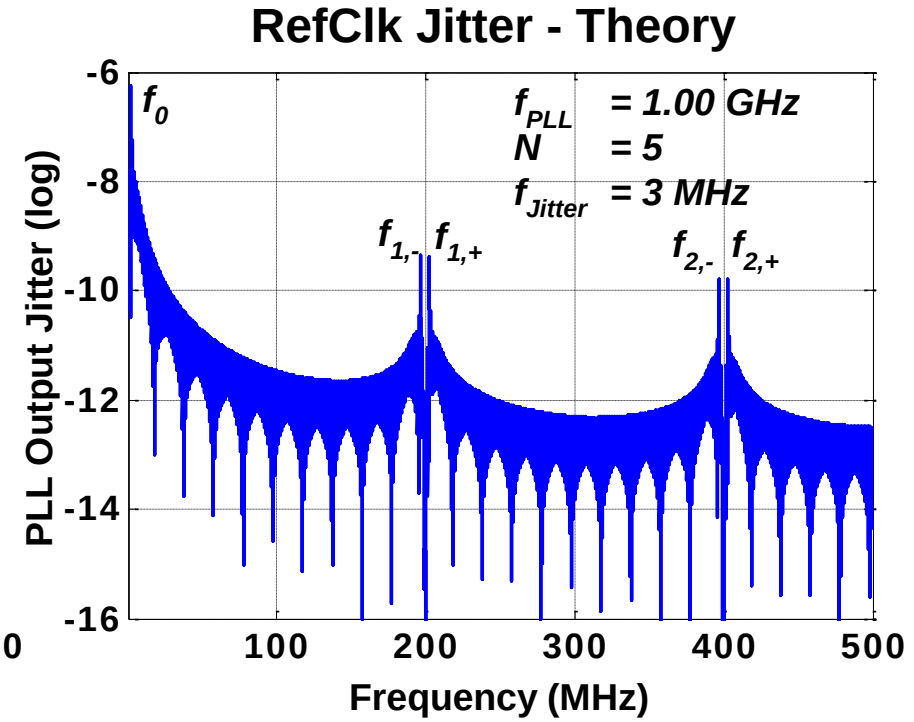


Effects cannot be captured by time-invarant model!

Theory vs. Simulation – Discrete-Time

RefClk Sinusoidal Jitter:





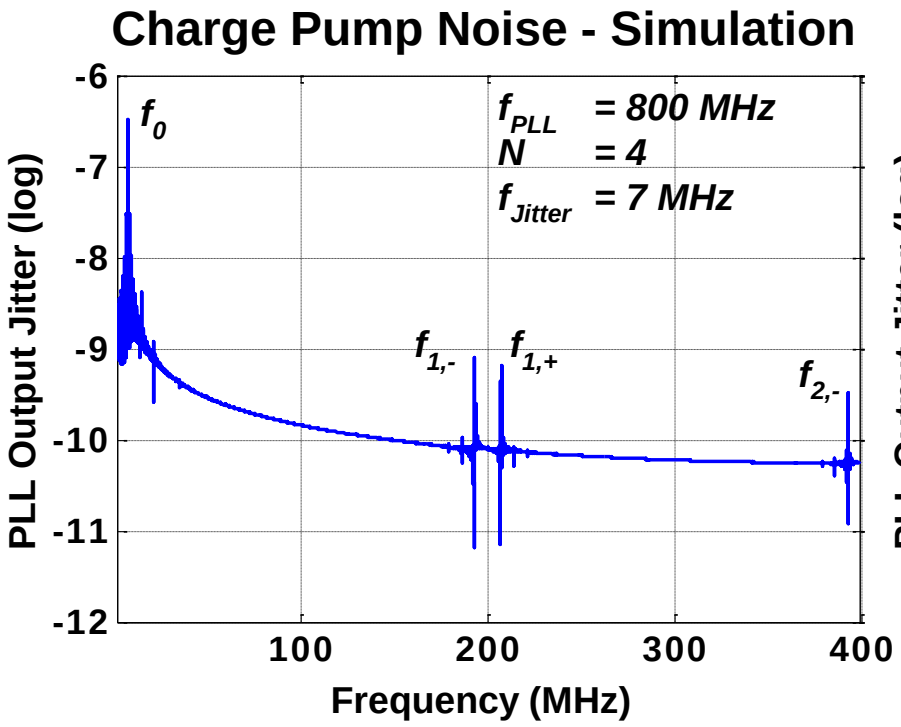
-Images produce *N*-1 additional spurs.

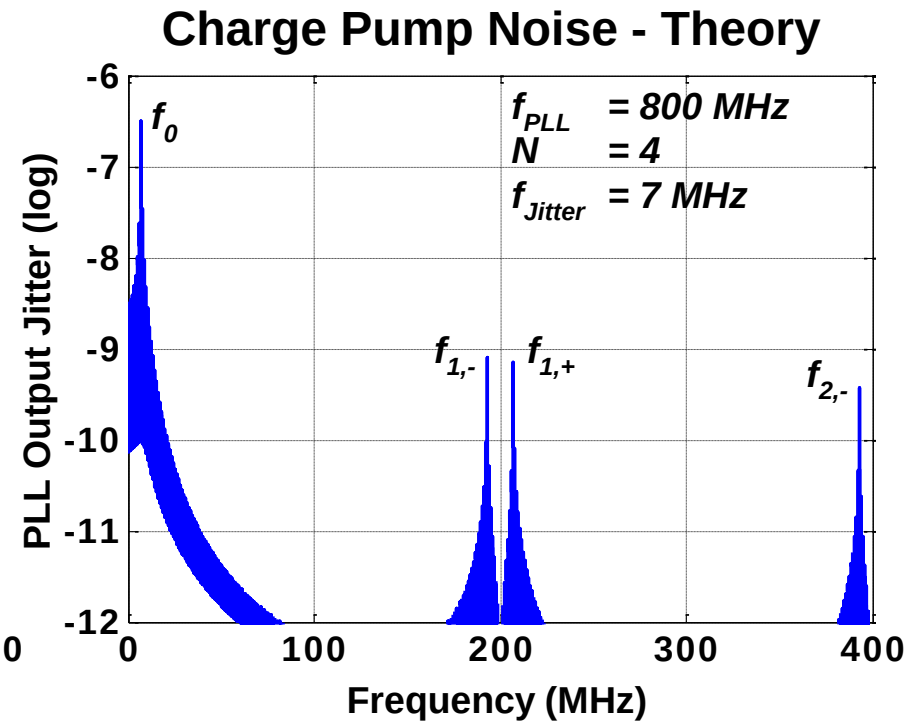
-Agreement between theory and simulation:

~1% for main spur, ~15% for secondary spurs.

Theory vs. Simulation – Discrete-Time

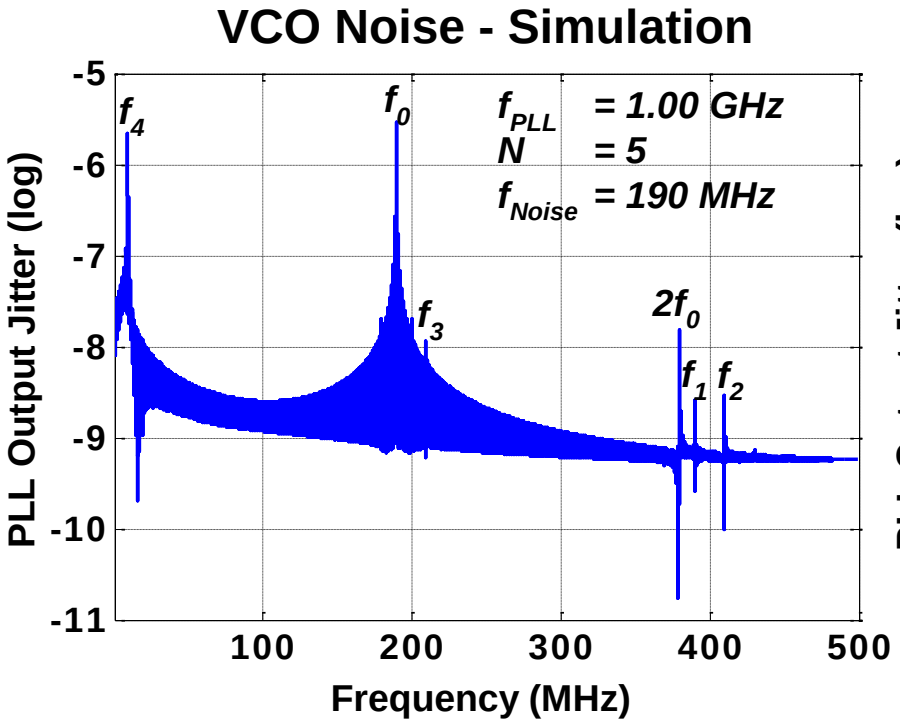
Charge Pump Sinusoidal Supply Noise:

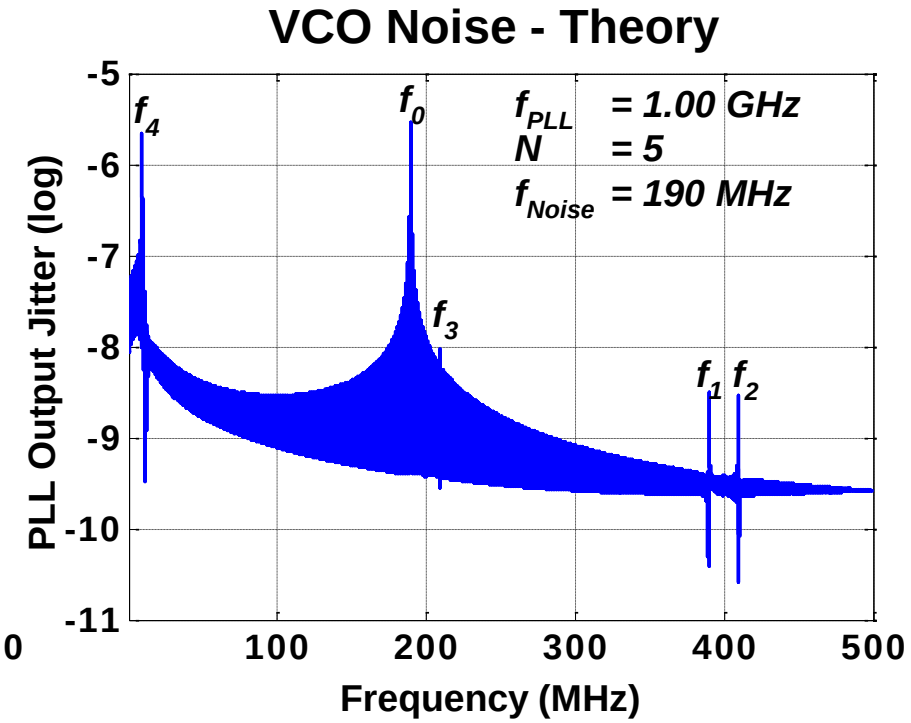




Theory vs. Simulation – Discrete-Time

VCO Sinusoidal Supply Noise:



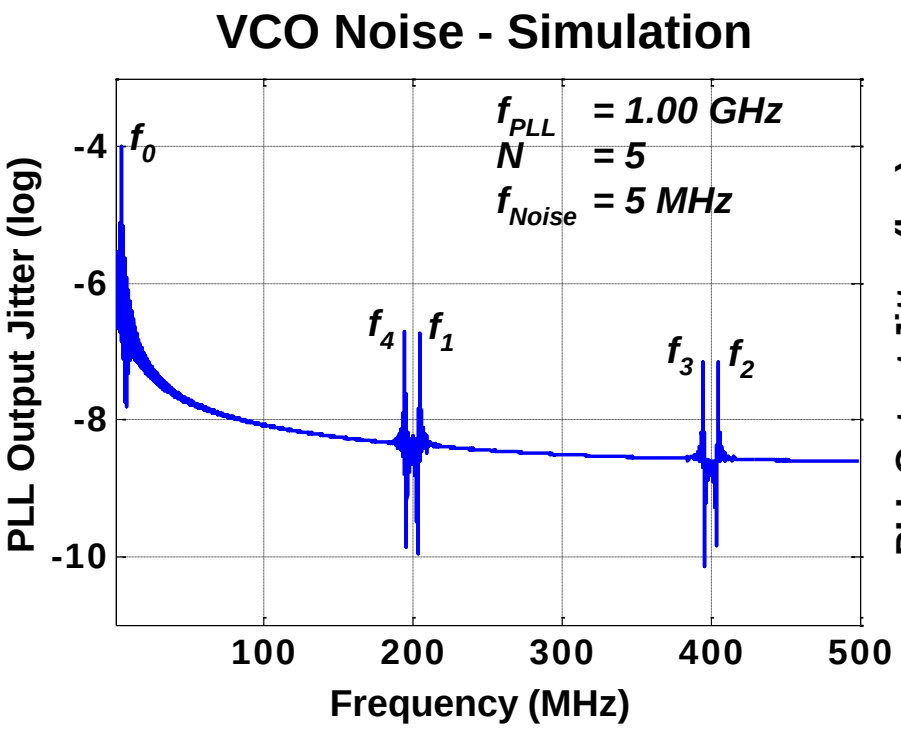


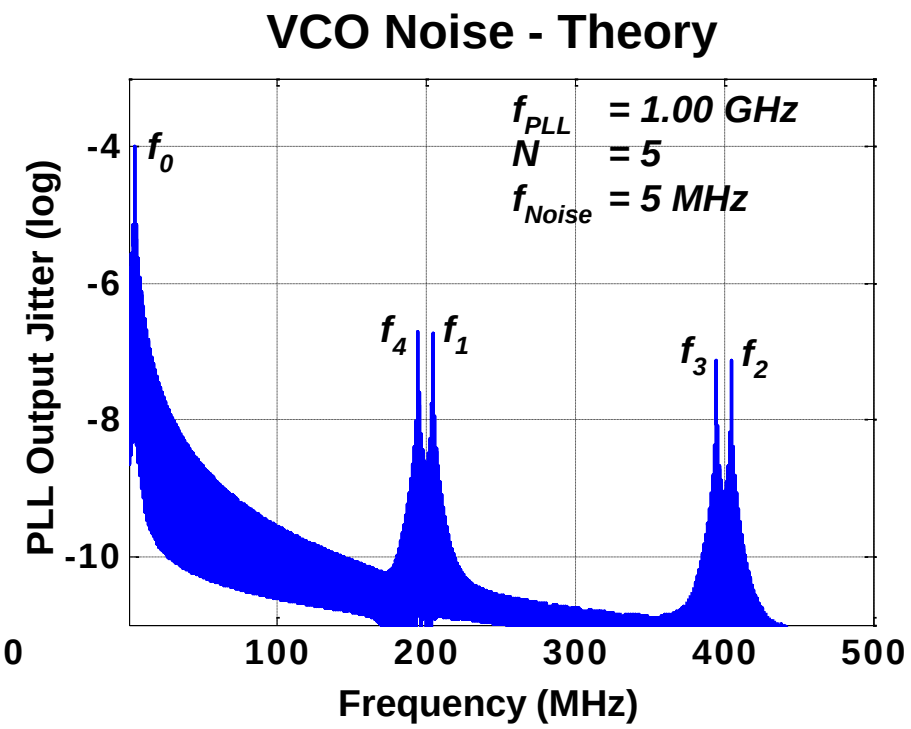
-Due to aliasing spur falls in-band (f_4=10 MHz).

-Simulation harmonic @ 380 MHz is not predicted by theoretical linear model.

Theory vs. Simulation – Discrete-Time

VCO Sinusoidal Supply Noise:





Effects cannot be captured by continuous-time model!

Conclusions

- Discrete-time, linear, cyclostationary model for PLL jitter was developed.
- Theoretical analysis results are compared to simulation model of the PLL implemented in Verilog-A.
- Theory agrees well with simulation and correctly predicts
  - Cyclostationary behavior of PLL
  - Frequency aliasing & images due to discrete-time nature of jitter