PLL On-Chip Jitter Measurement: Analysis and Design

Socrates D. Vamvakos[1], Vladimir Stojanović[2], Jared L. Zerbe[3], Carl W. Werner[3], Don Draper[3], Borivoje Nikolić[1]

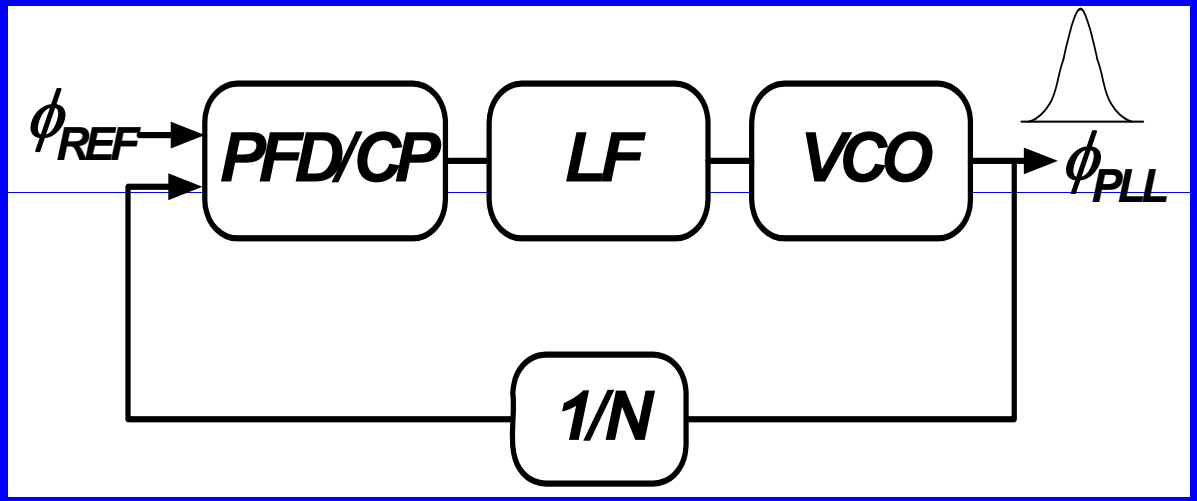
[1]University of California, Berkeley

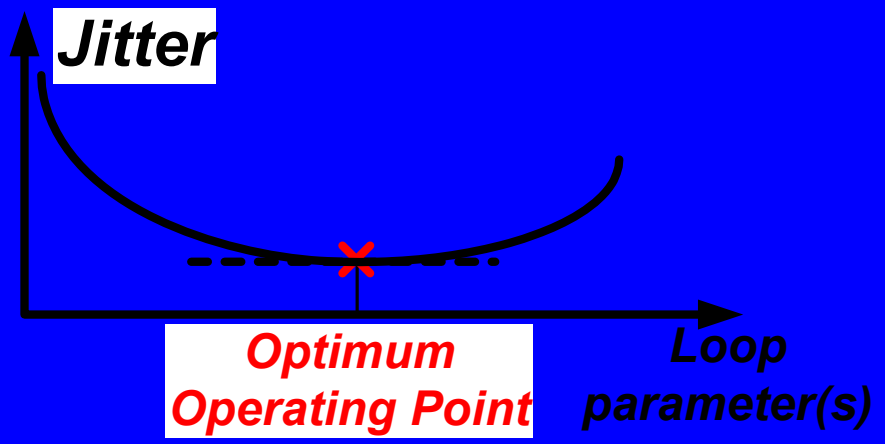
[2] M.I.T.

[3] Rambus, Inc.

PLL Jitter Optimization

- Minimum jitter can be achieved by adjusting loop parameters (ω_N, ζ).

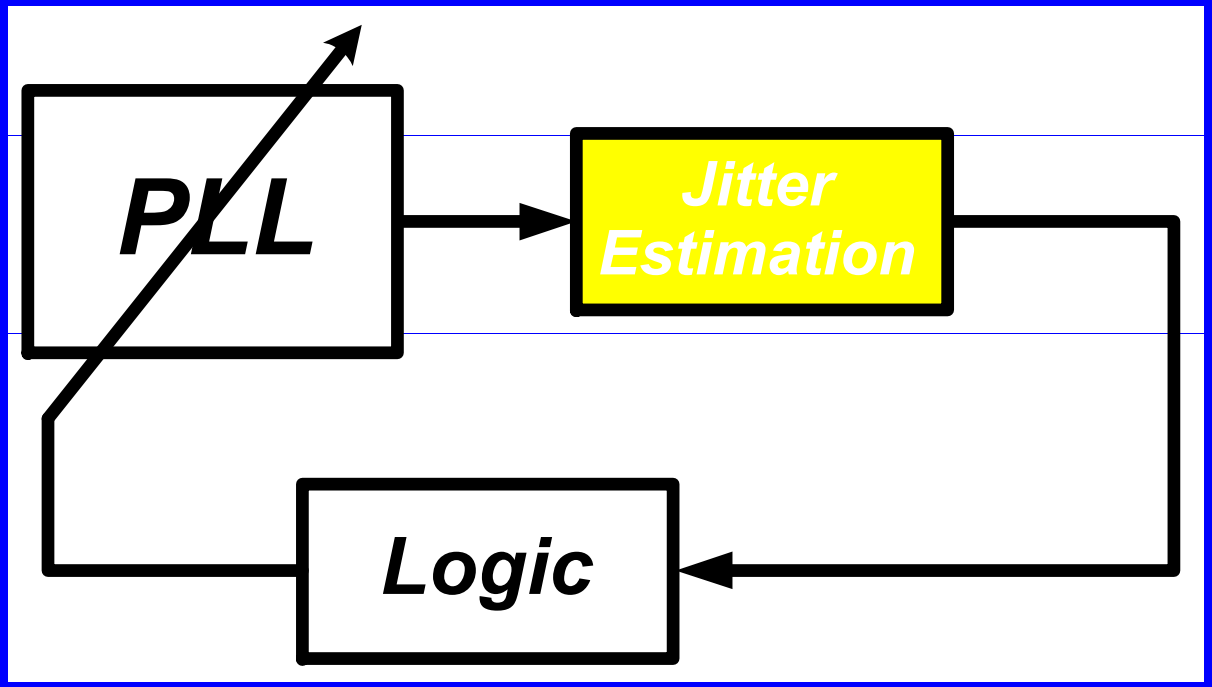




- Objective: Operate at minimum jitter point

PLL Jitter Optimization

- Adaptive scheme can compensate for:
  - PVT variations
  - Unknown noise environment
  - Different operating frequencies



Jitter estimation critical for correct operation

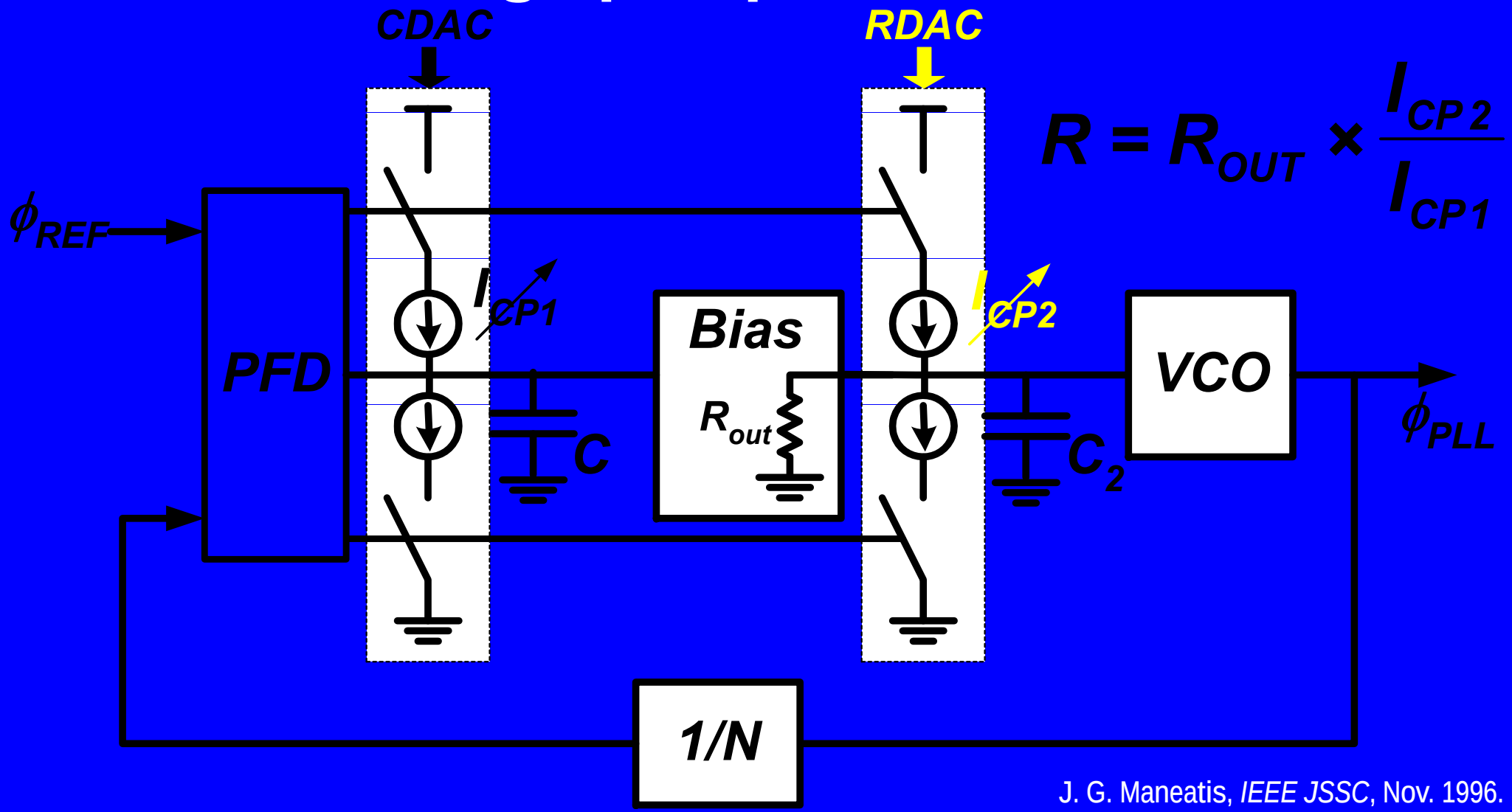
M. Mansouri et al, *IEEE Trans. Circuits Syst. II*, Nov. 2003.

Outline

- Motivation
- System Implementation
  - PLL circuit
  - Jitter Estimation Methods
    - Dead-Zone Algorithm
    - Variance Metric Algorithm
- Measurement Results
  - Error Sources
- Conclusions

PLL Circuit

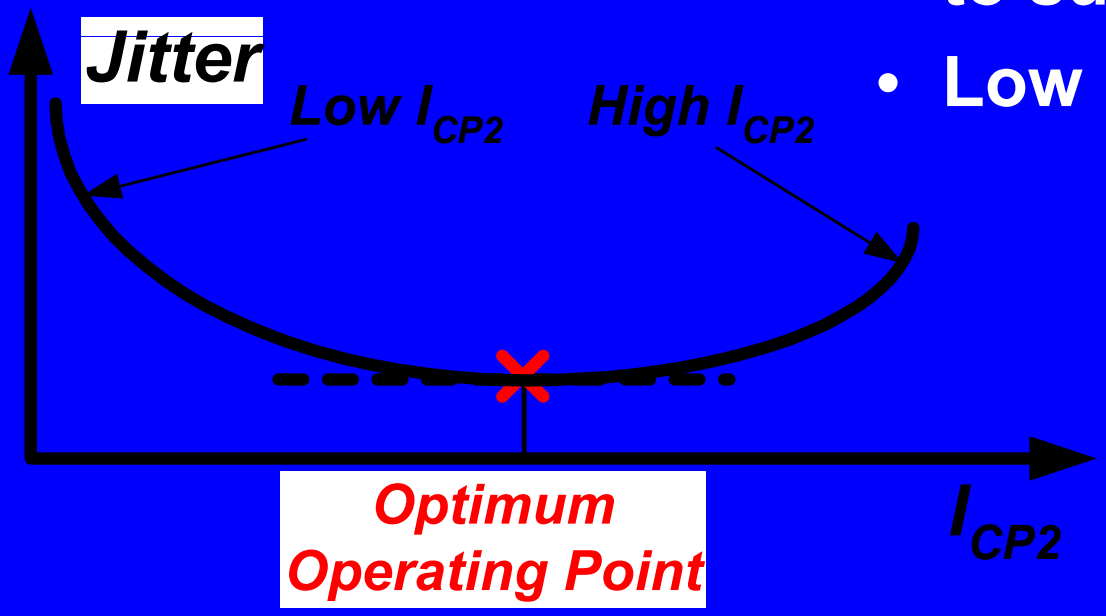
- Dual charge pump, self-biased PLL



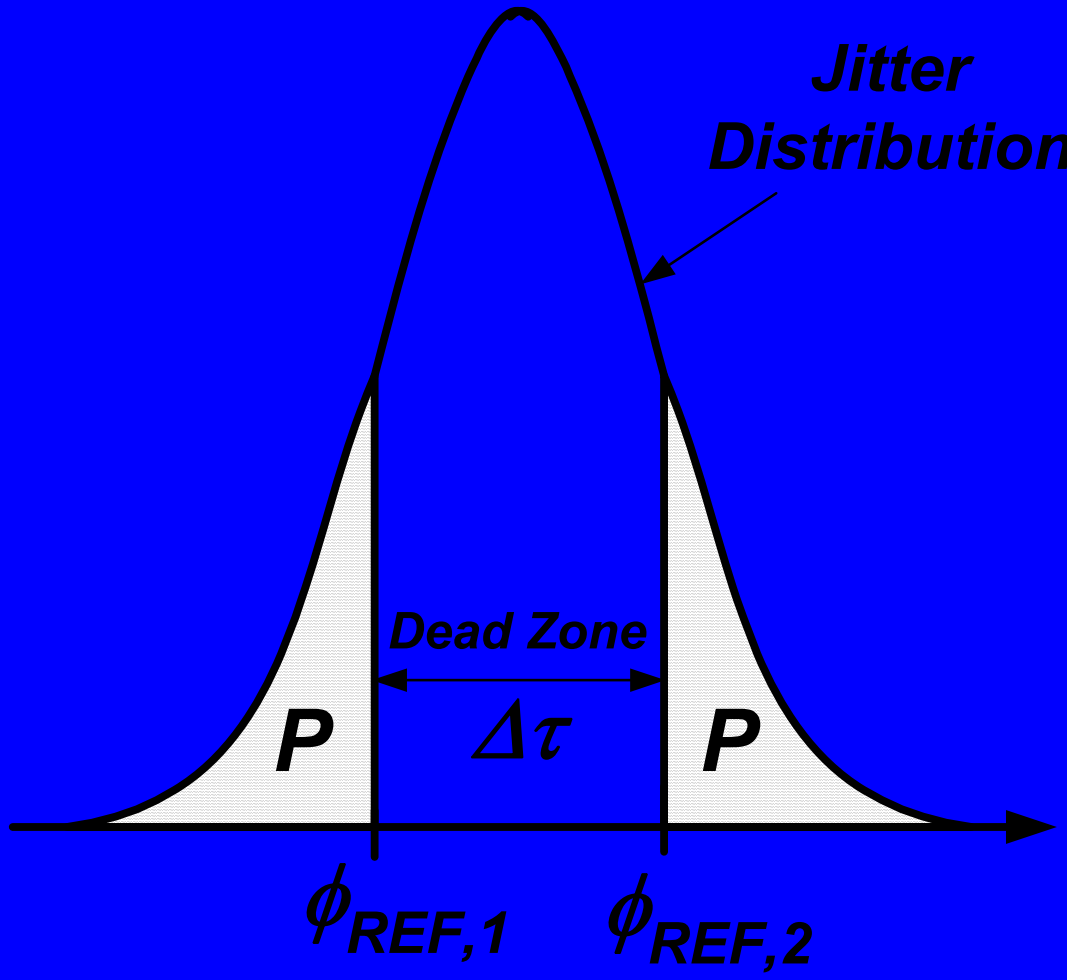
J. G. Maneatis, *IEEE JSSC*, Nov. 1996.

PLL Circuit

- Modulate PLL jitter by changing I_{CP2}
- Low I_{CP2}
  - Low damping factor ζ
  - Jitter peaking
- High I_{CP2}
  - High self-generated periodic jitter
  - High charge pump sensitivity to supply noise
  - Low phase margin



Dead-Zone Jitter Estimation

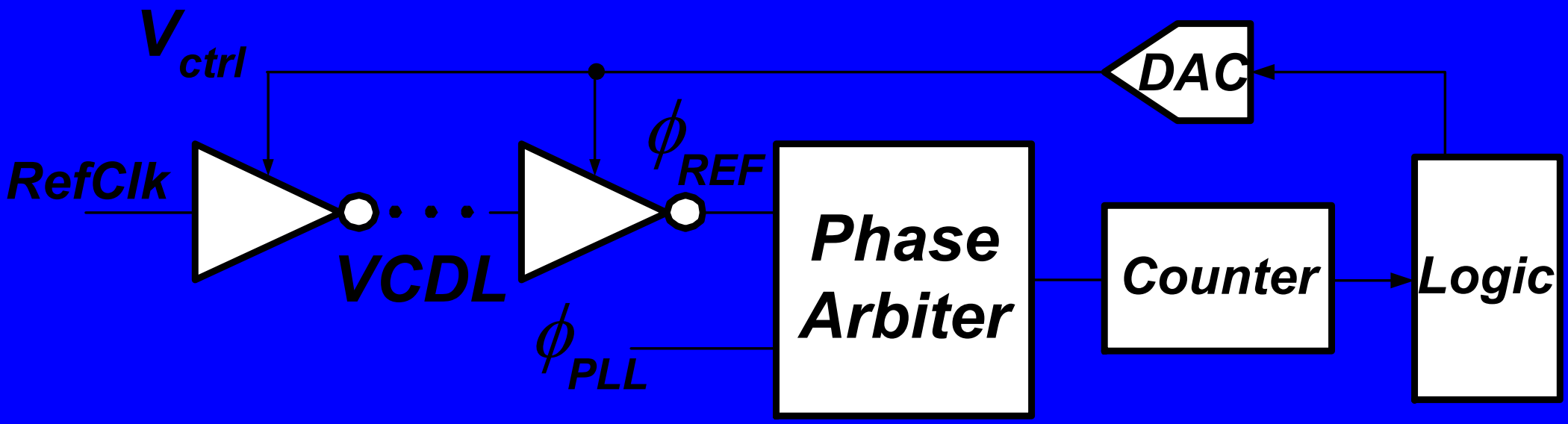


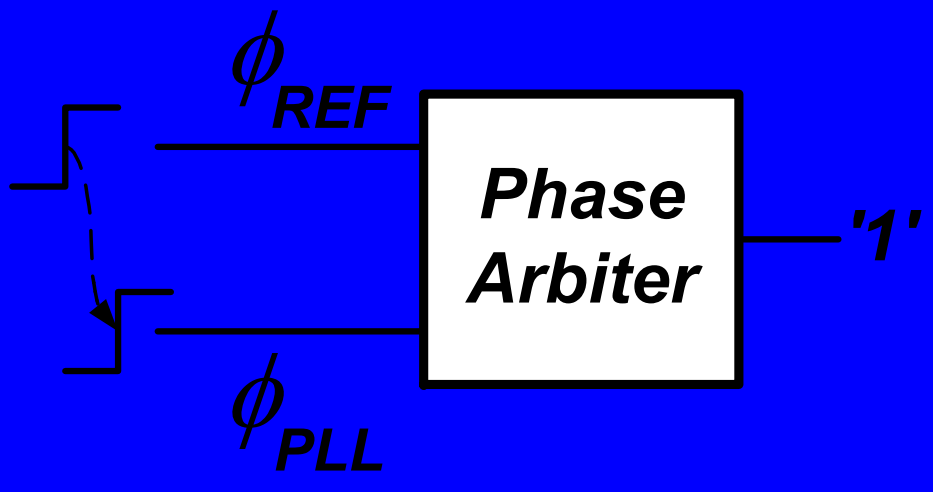
- **Find boundaries of jitter distribution for tail probability *P*.**

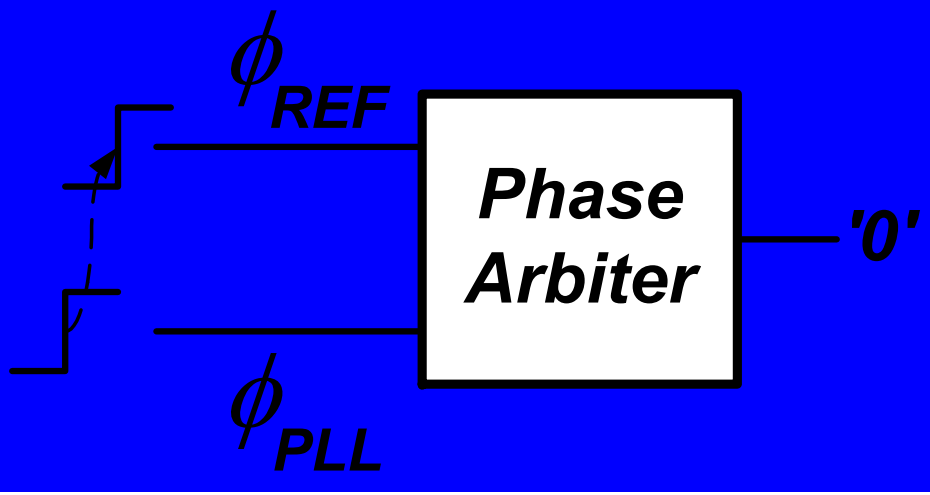
Y. Moon et al., *IEEE JSSC*, Dec. 2001.

Dead-Zone Jitter Estimation

- Measurement circuit

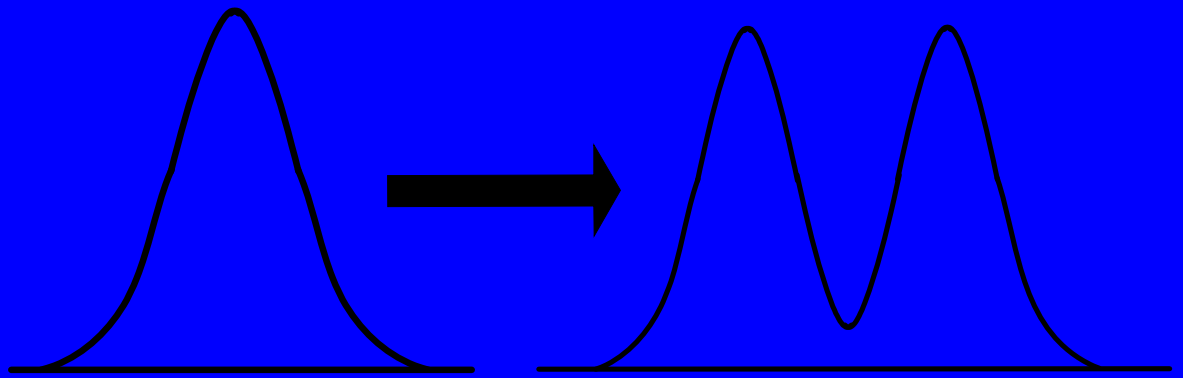






Dead-Zone Jitter Estimation

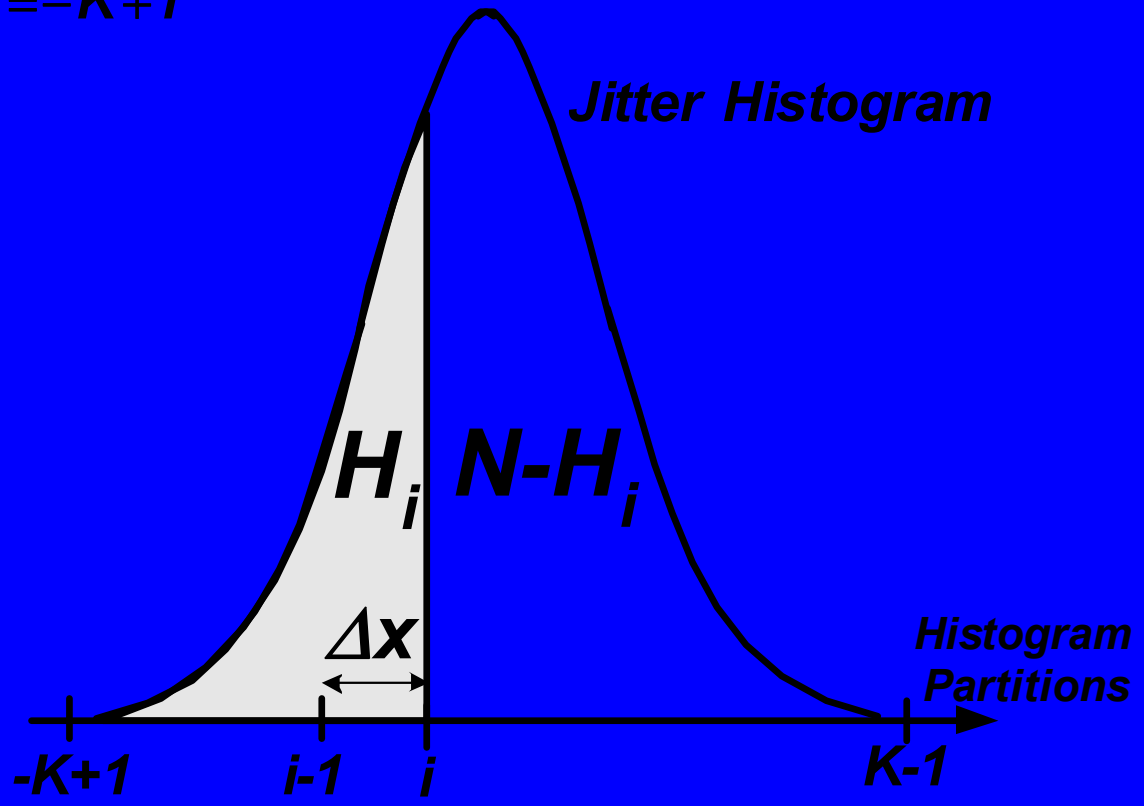
- **Possible issues:**
  1) **Shape of jitter distribution must be known**
  2) **Non-Gaussian jitter distribution**
     - **E.g.: Increased periodic jitter and/or loop instability cause bimodality**



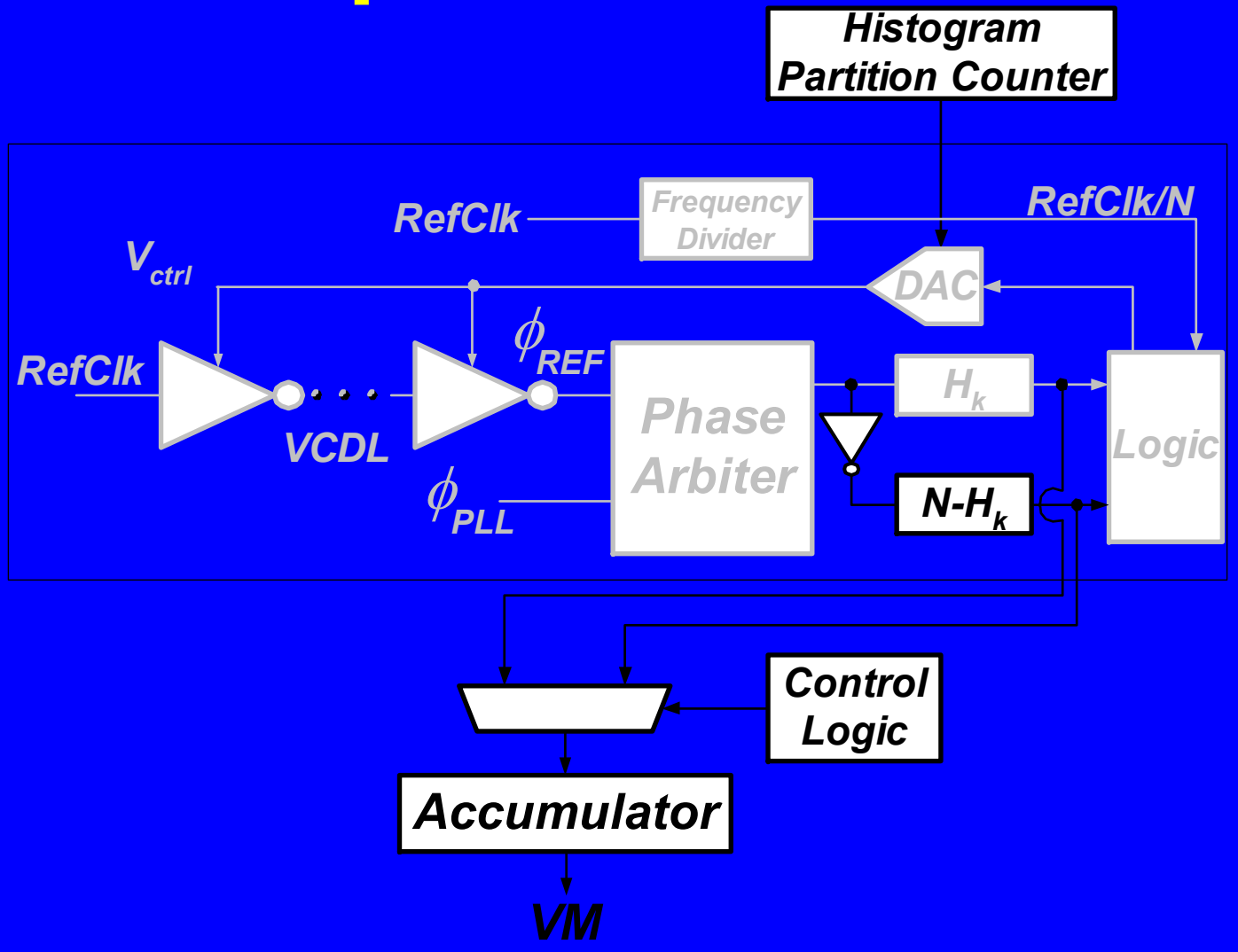
Variance Metric Jitter Estimation

- Combine measurements along jitter histogram to compute variance metric

$$VM = \sum_{i=-K+1}^{K-1} \left[(K - i) \cdot H_i + (i + K) \cdot (N - H_i) \right]$$

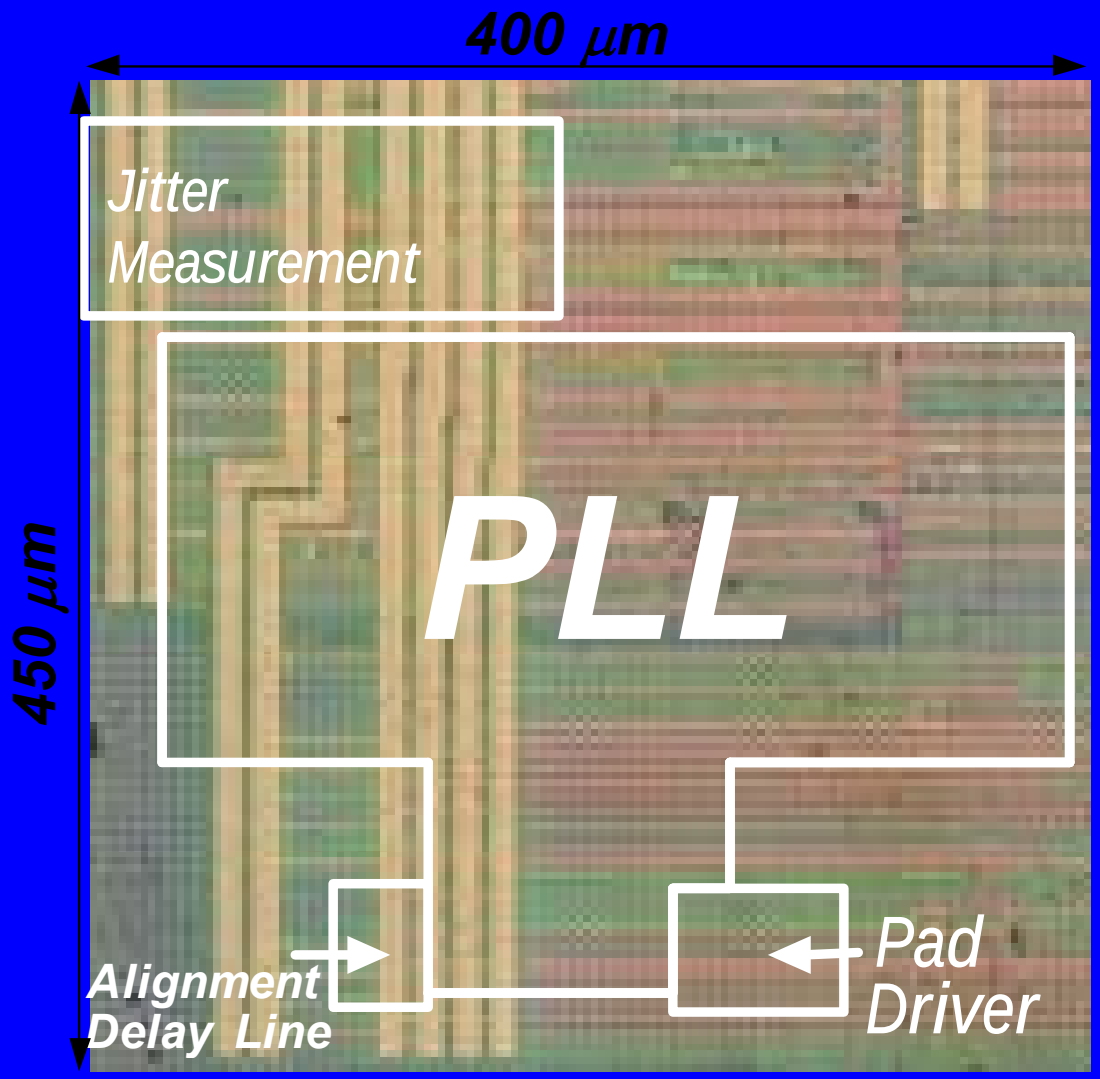


Circuit Implementation



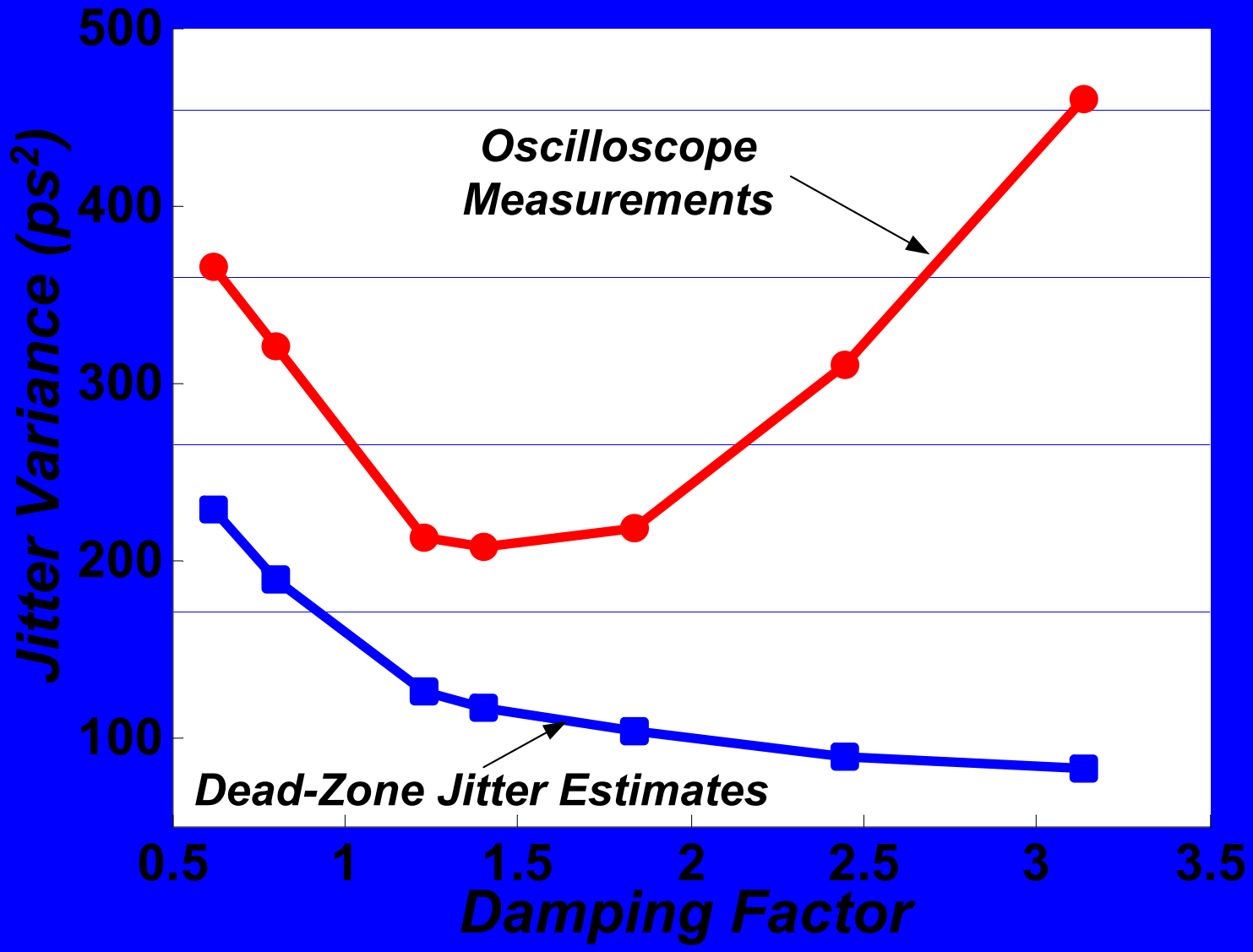
- Simple extension of dead-zone circuit
- No multiplication required

System Implementation



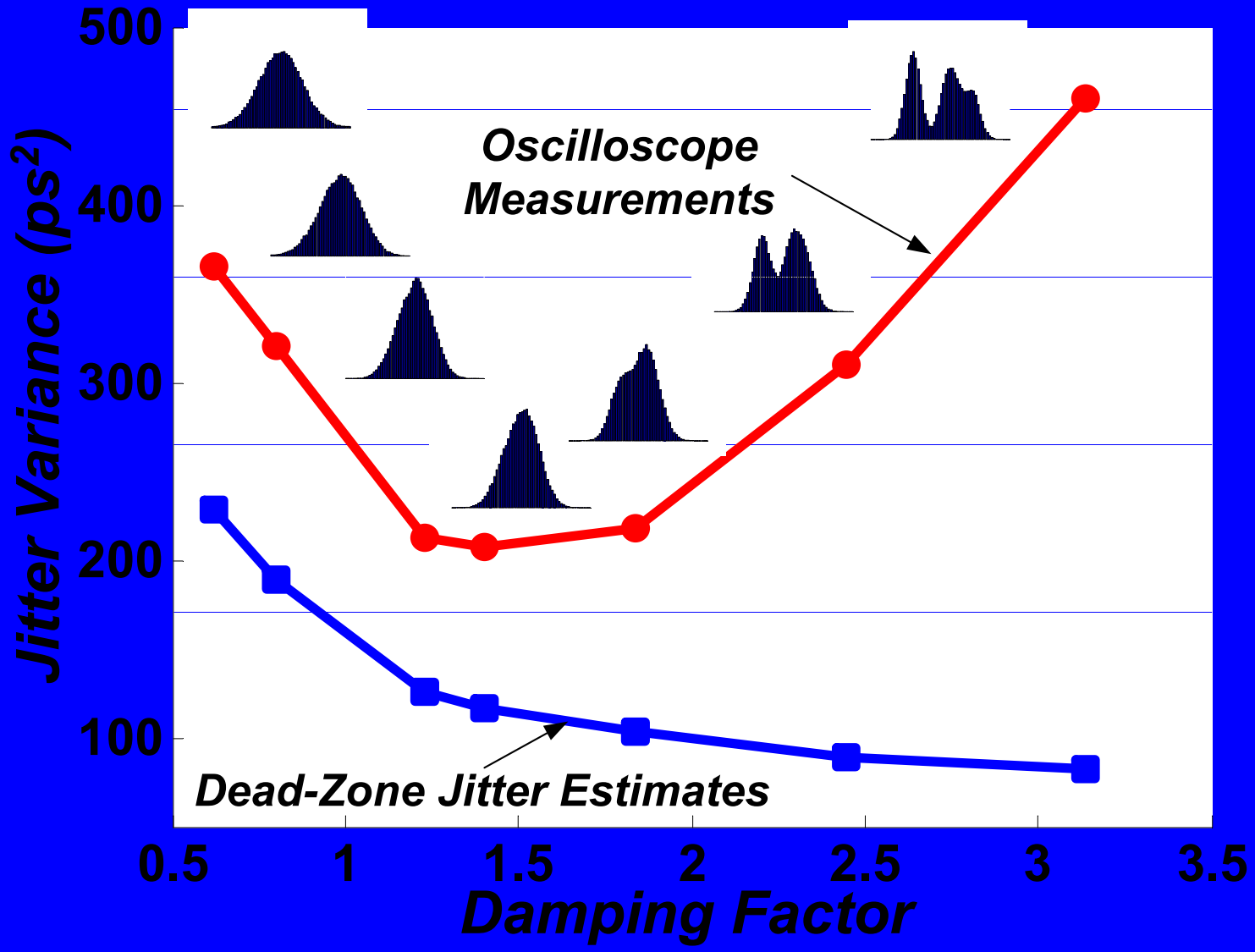
- 0.13 μm CMOS
- PLL: 17 mW (1GHz)
- Meas. Ckt: 10 mW

Measurement Results



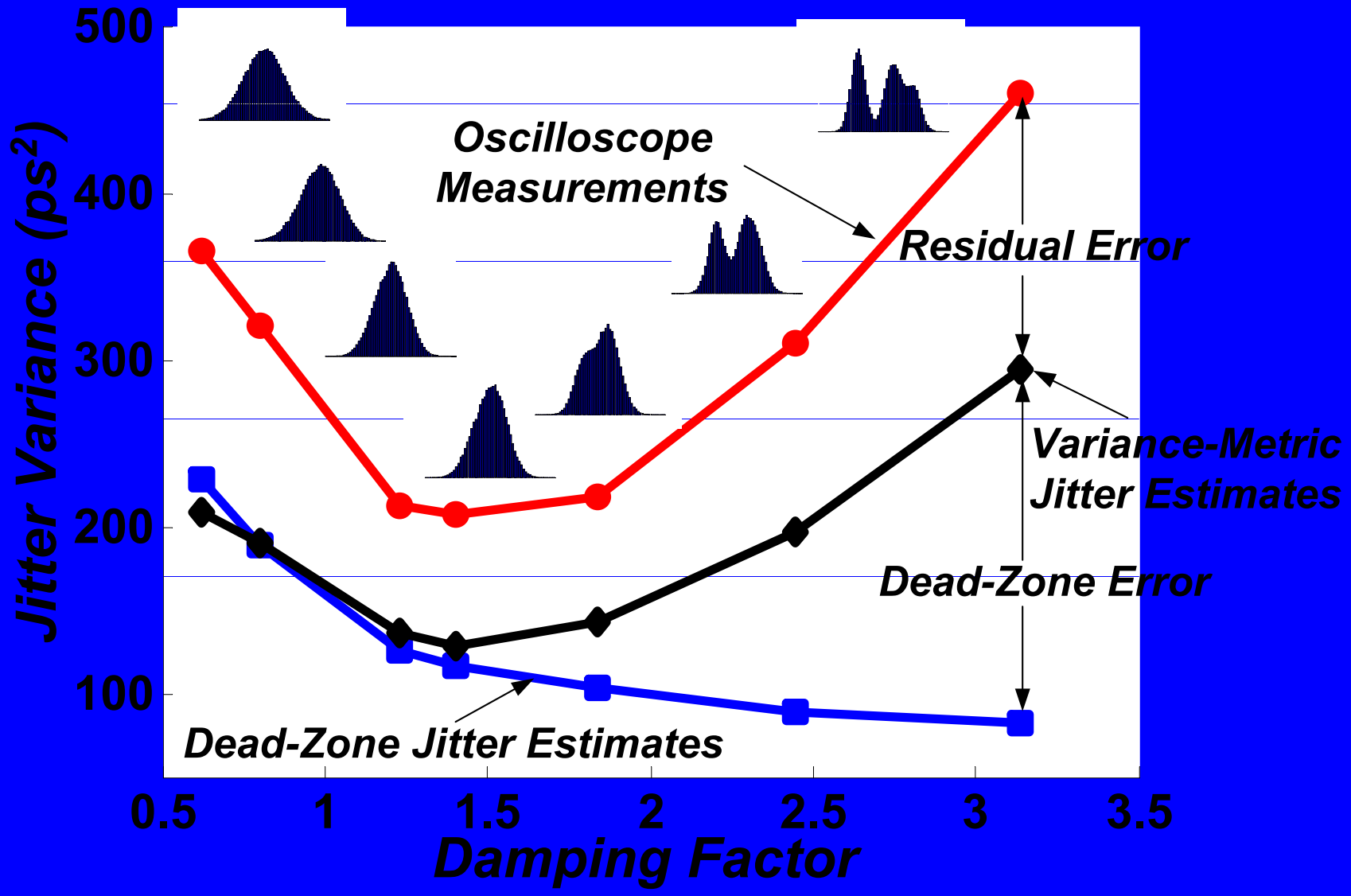
- Large error for high damping factors

Measurement Results



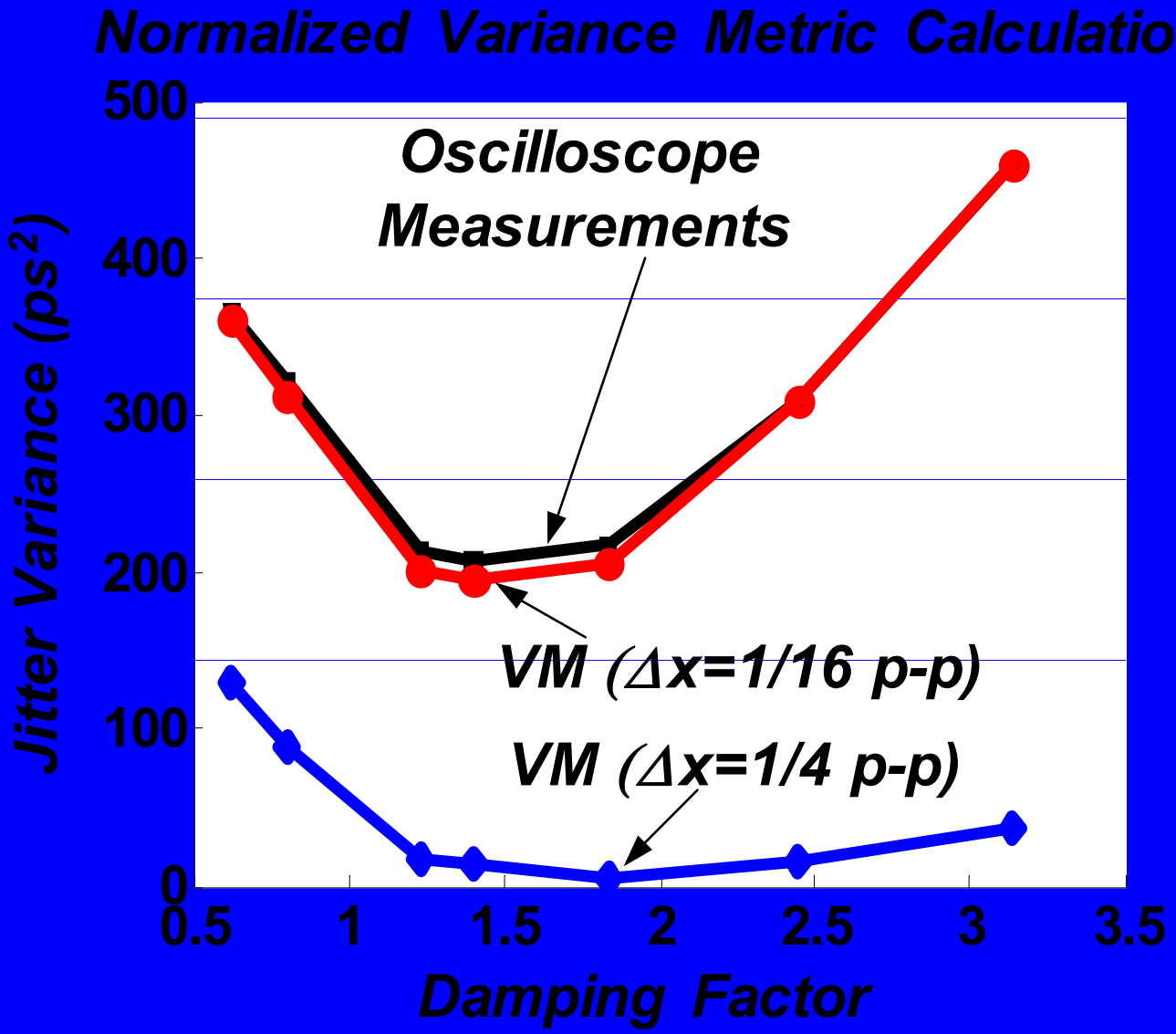
- Bimodal distibution due to increased periodic jitter

Measurement Results



- Variance metric identifies minimum

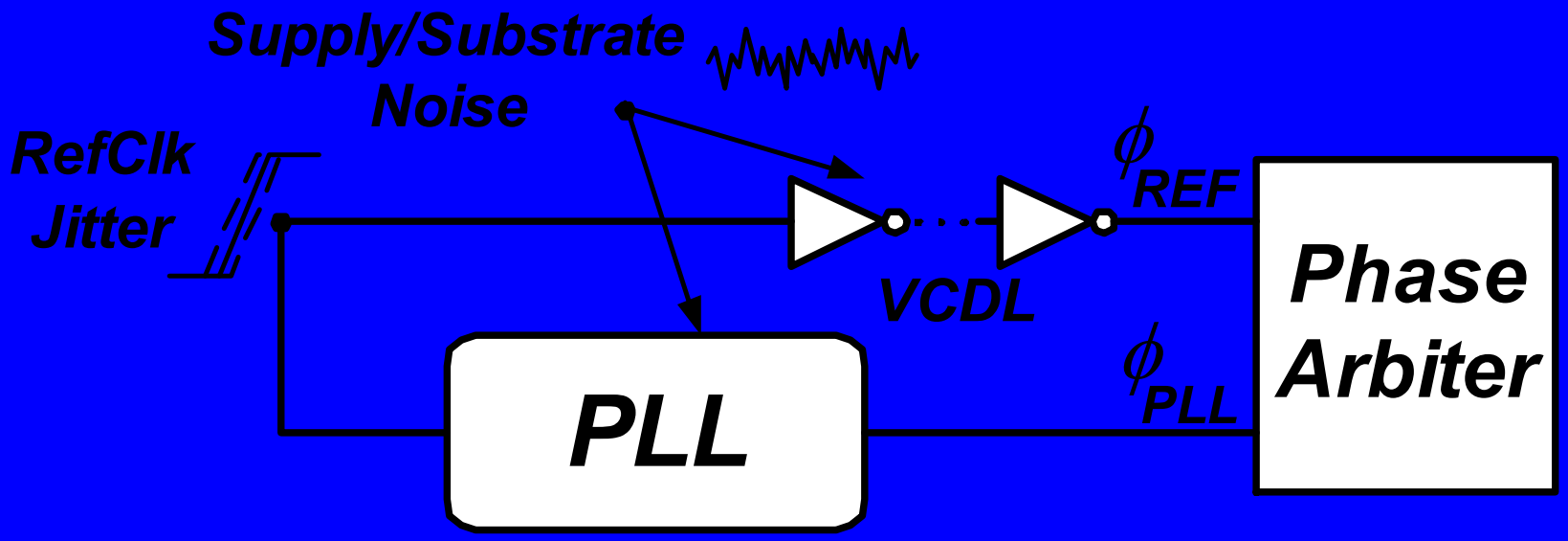
Variance Metric Performance



- Smaller Δx improves jitter estimates

Residual Error

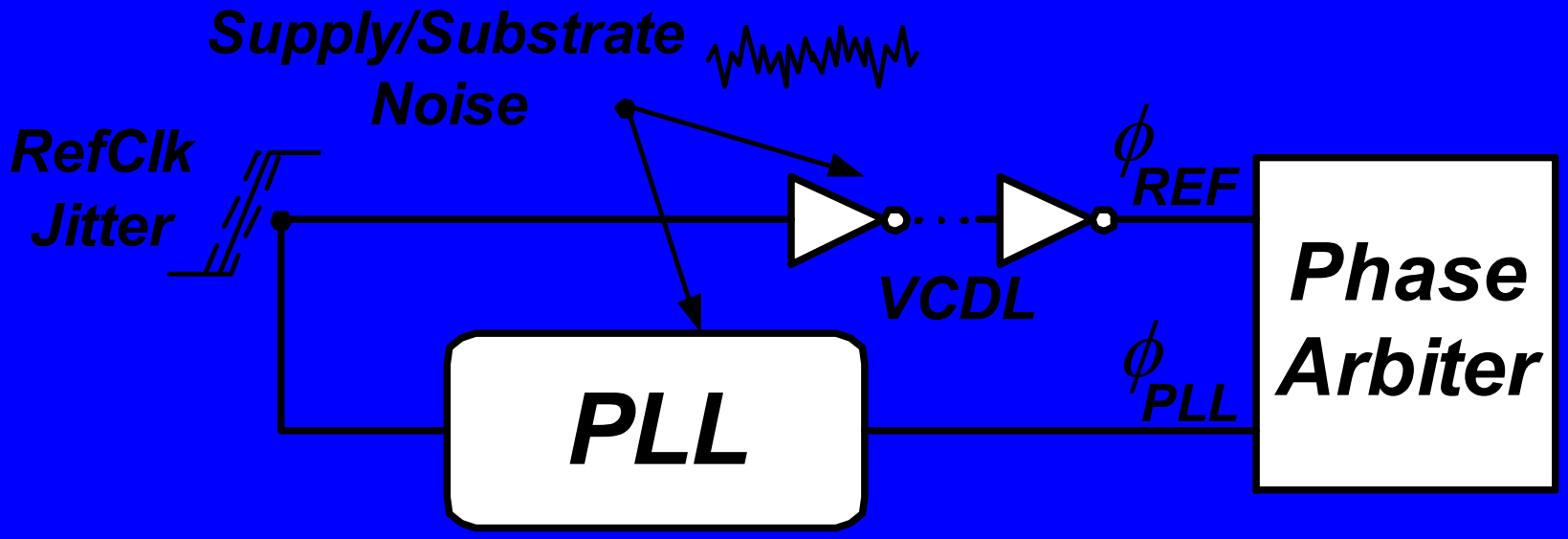
- Source: Correlated supply/substrate noise and RefClk jitter



$$Var[\varphi_{PLL} - \varphi_{REF}] = Var[\varphi_{PLL}] + Var[\varphi_{REF}] - 2 \times Cov[\varphi_{PLL}, \varphi_{REF}]$$

Residual Error

- Source: Correlated supply/substrate noise and RefClk jitter

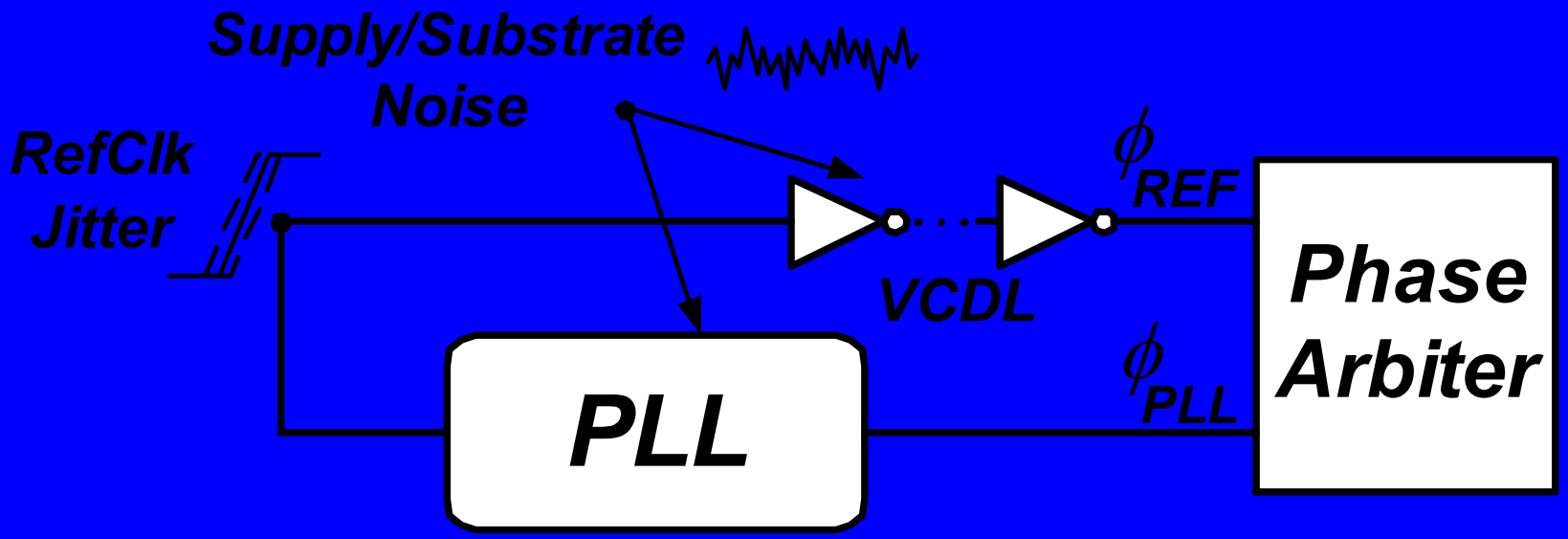


$$Var[\varphi_{PLL} - \varphi_{REF}] = Var[\varphi_{PLL}] + Var[\varphi_{REF}] - 2 \times Cov[\varphi_{PLL}, \varphi_{REF}]$$

PLL Jitter

Residual Error

- Source: Correlated supply/substrate noise and RefClk jitter

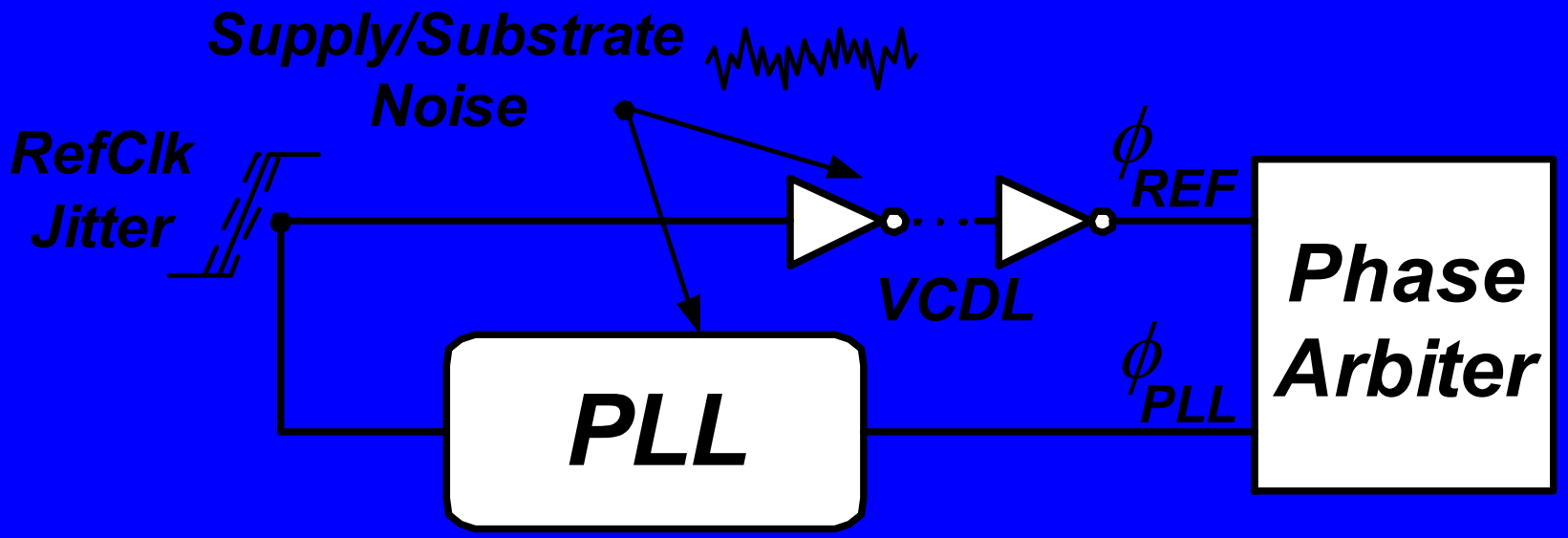


$$Var[\varphi_{PLL} - \varphi_{REF}] = Var[\varphi_{PLL}] + Var[\varphi_{REF}] - 2 \times Cov[\varphi_{PLL}, \varphi_{REF}]$$

Constant

Residual Error

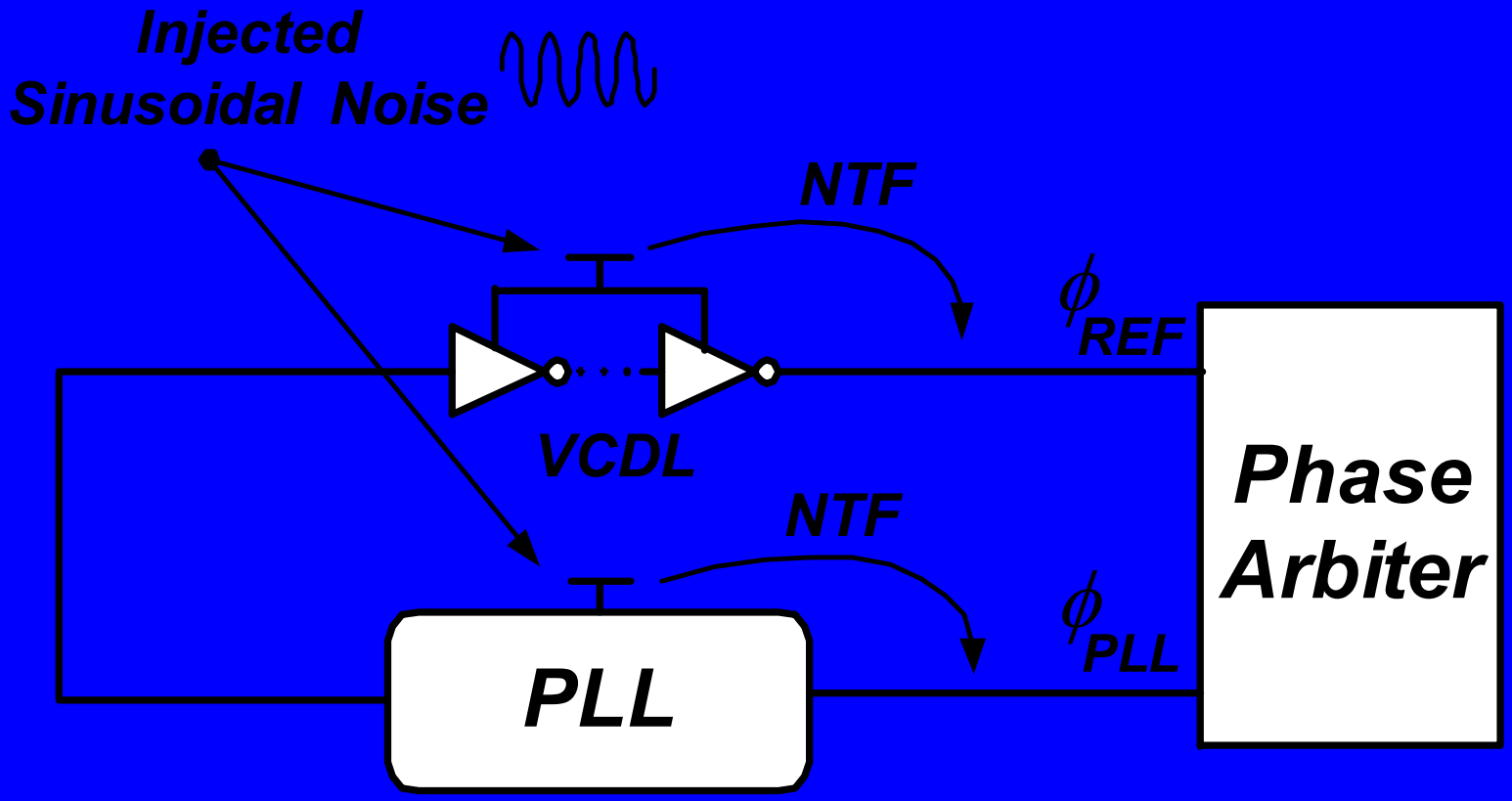
- Source: Correlated supply/substrate noise and RefClk jitter



$$Var[\varphi_{PLL} - \varphi_{REF}] = Var[\varphi_{PLL}] + Var[\varphi_{REF}] - 2 \times Cov[\varphi_{PLL}, \varphi_{REF}]$$

Dependent on PLL operating point

Calculation of Correlation Error



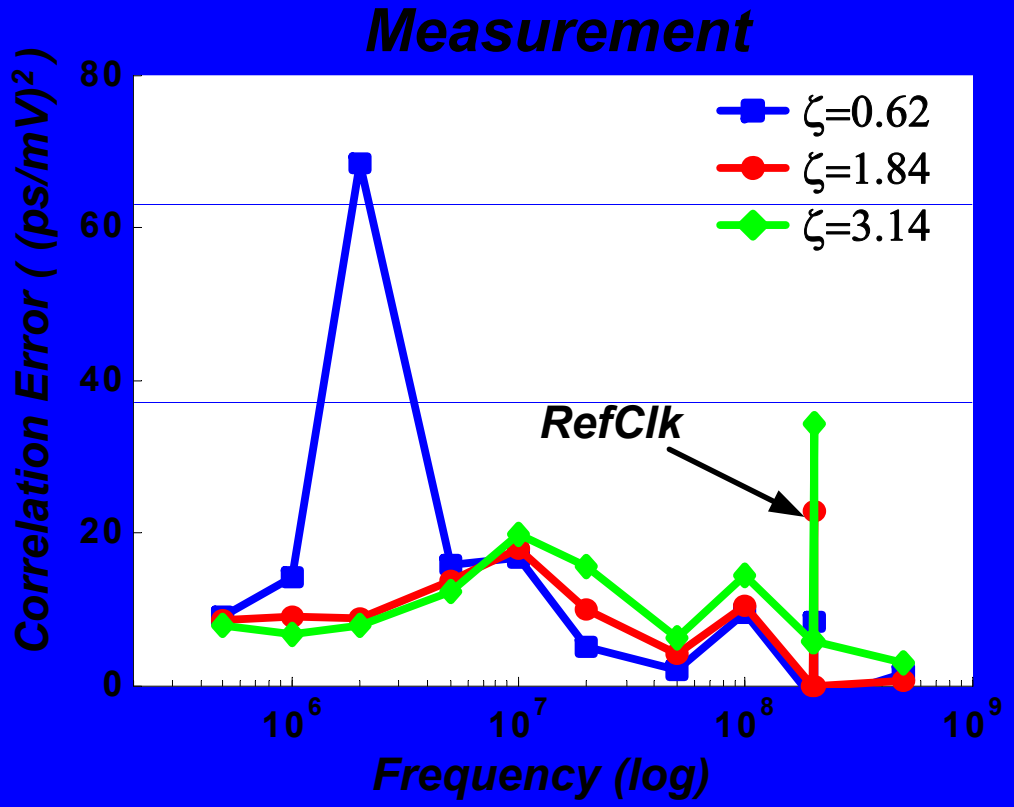
- **Measurement: Solve for correlation error**

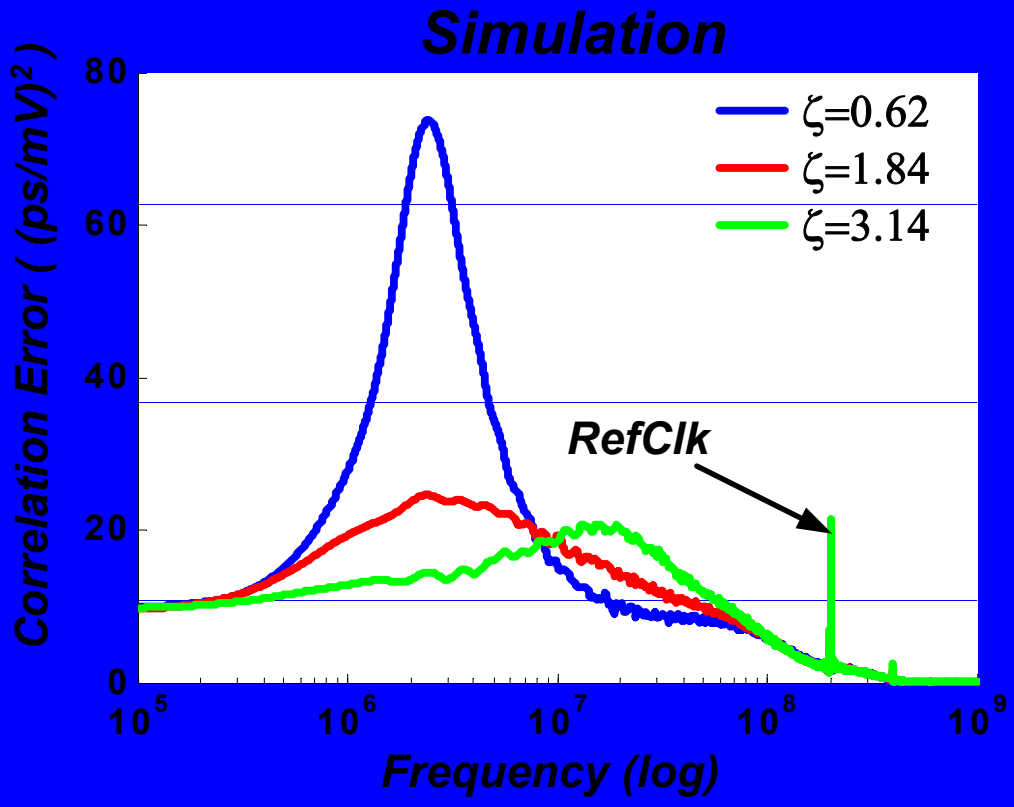
$$2 \times Cov[\varphi_{PLL}, \varphi_{REF}] = Var[\varphi_{PLL} - \varphi_{REF}] - Var[\varphi_{PLL}] - Var[\varphi_{REF}]$$

- **Simulation: Use noise transfer functions (NTF)**

Correlation Error vs. Frequency

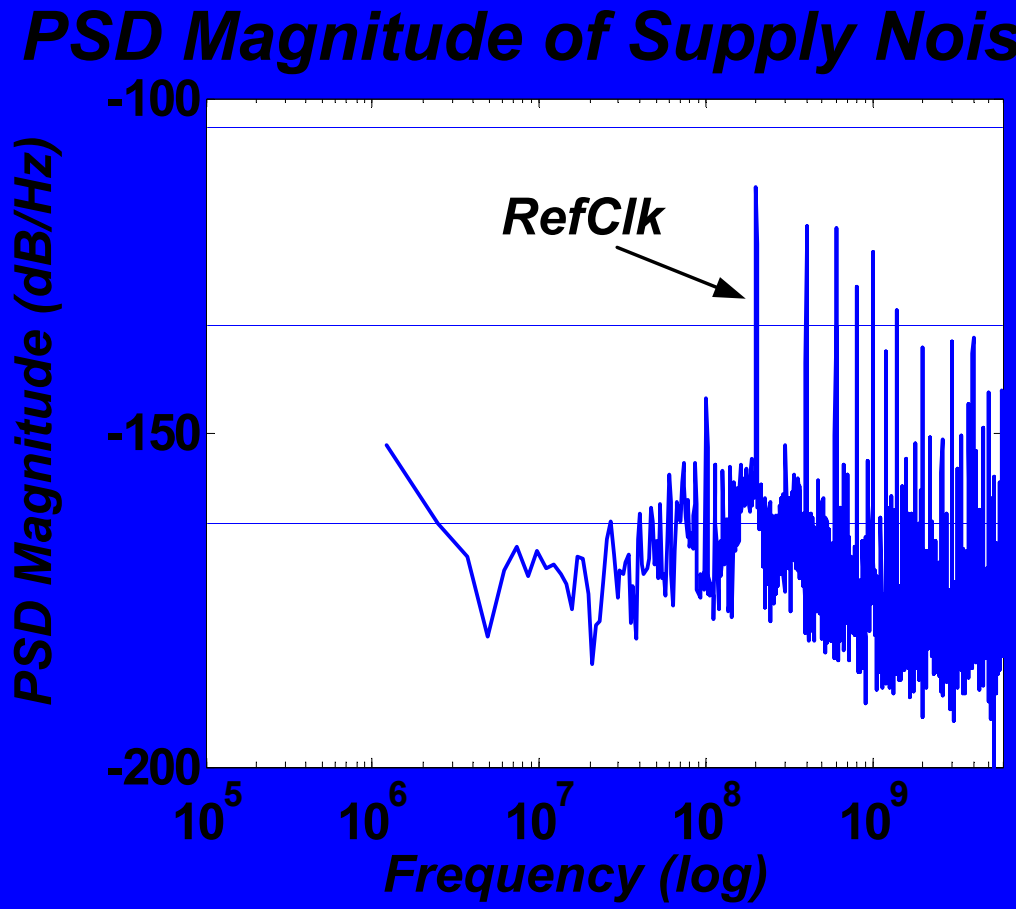
Normalized Supply Correlation Error (Abs. Value)

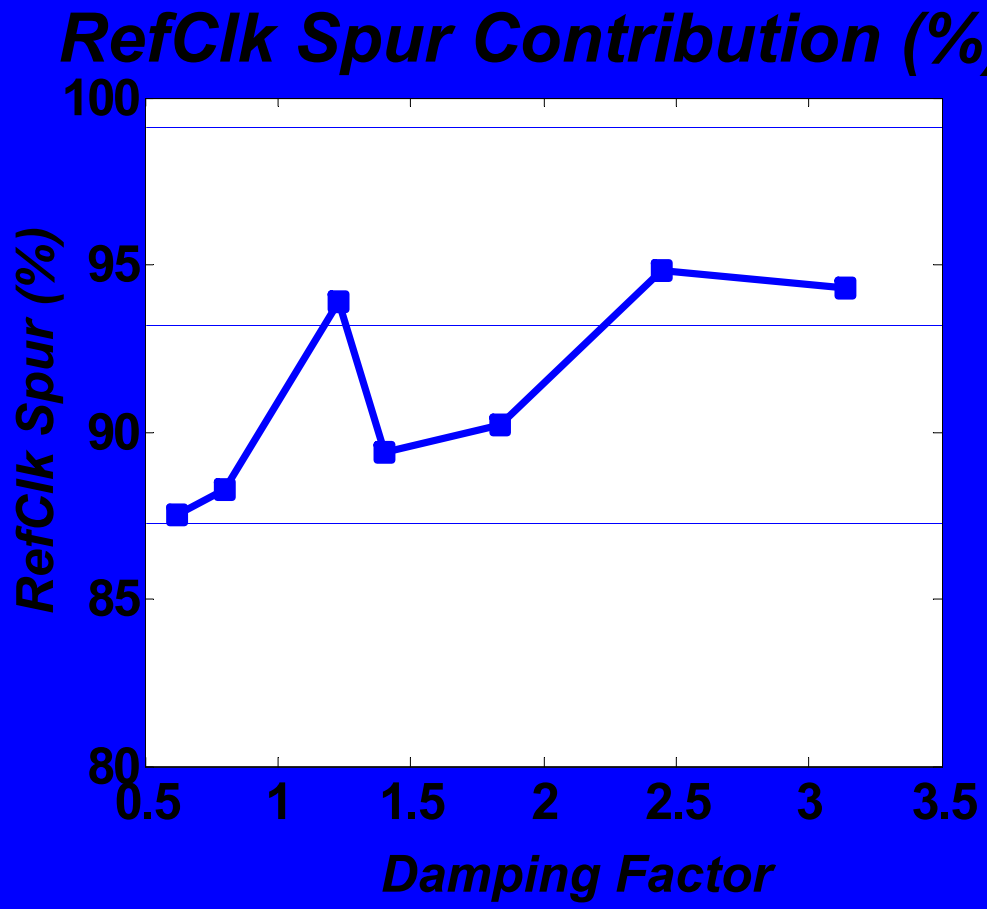




- **Total error: Multiply with supply noise PSD and integrate over all frequencies**
- **Same analysis for RefClk correlation error**

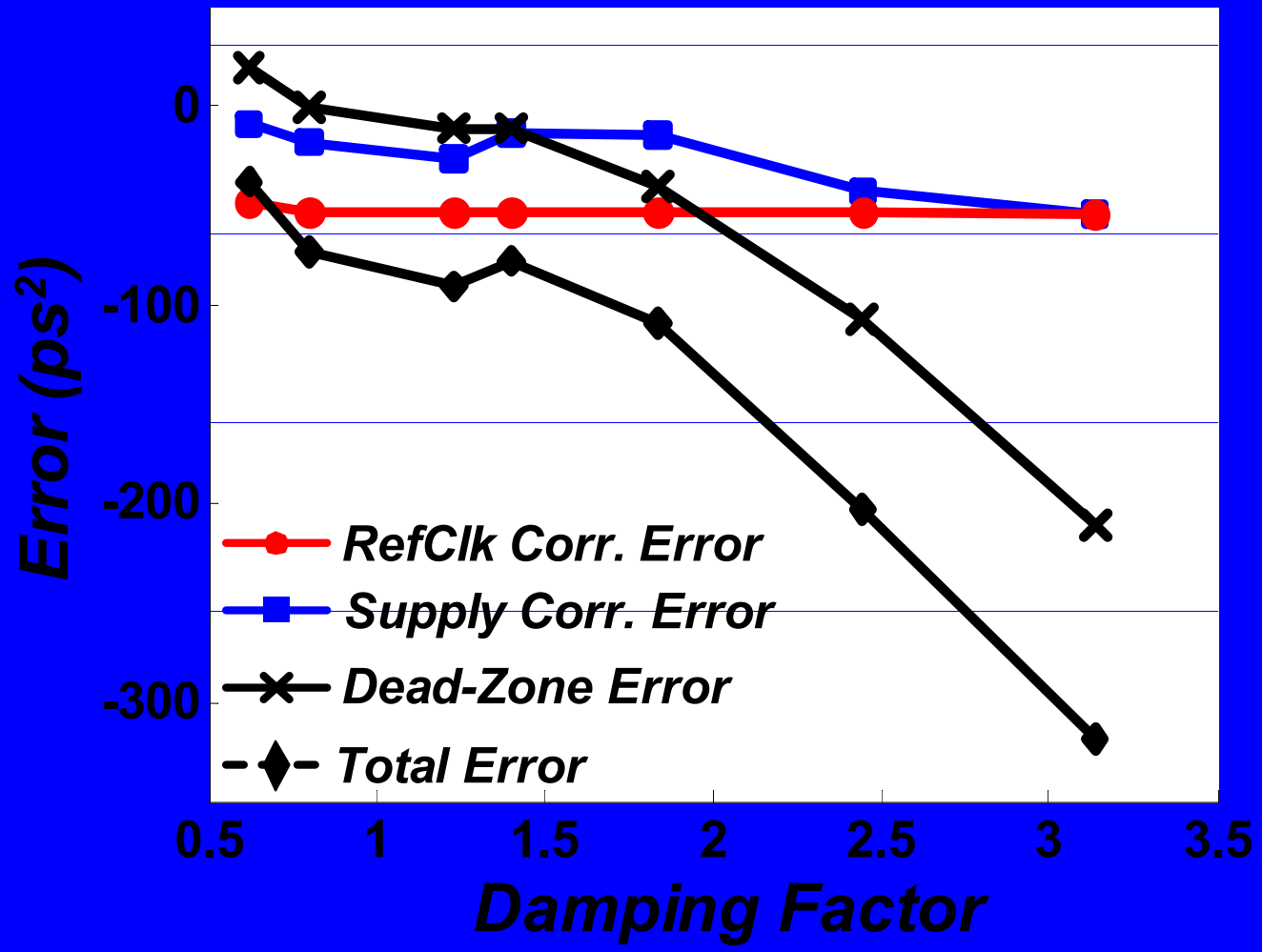
Supply Correlation Error





- RefClk spur contributes ~90% of supply correlation error

Measurement Error Components



- Relative jitter values affected mostly by dead-zone error

Conclusions

- Study of on-chip jitter estimation methods
- Sources of measurement error
  - Dead-zone algorithm
  - Correlated noise sources
- Proposed design improvements
  - Variance metric algorithm
    - Correct operation for any jitter distribution