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The Research Laboratory of Electronics at the Massachusetts Institute of Technology

Chipping Away at VLSI COMPUTER-AIDED DESIGN

In search of enlightenment, medieval theologians posed the question, "How many angels can dance on the head of a pin?" Today, faced with a similar but more mundane paradox, computer experts seek an answer to the question, "How many transistors can fit on a microchip?" As semiconductor materials and processing technologies have advanced, electronic components have become smaller, circuit arrays denser, microchips larger, and their functions faster and more complex. Scientists and engineers must now tame the rapid pace of this challenging technology by devising new design methods for integrated circuits that are quick, reliable, and economical.

Computer scientists, electrical engineers, mathematicians, materials scientists, and physicists are all engaged in the highly interdisciplinary field of integrated circuit design. Their investigations are driven, in part, by the quest for faster, more accurate, and more powerful digital computers. Conversely, these high-performance computers are the vehicles that transport researchers into still deeper and more fascinating areas of exploration.

It is simple to design a circuit that contains a few transistors, but the design of an entire system that uses thousands of transistors involves many designers who may work on different parts or stages of the design simultaneously. To be successful, a design team must possess an understanding of each level of design. Rarely does one person possess expertise at all levels, nor is the entire process achieved solely by human means. Without modern computer-

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An integrated circuit mask layout of the Intel 386 microprocessor (magnified 200 times) provides a backdrop for Professor Jonathan Allen. This computer-generated plot of the 386 chip, which contains 275,000 transistors, was part of a recent display at the MIT Museum, "Information Art: Diagramming Microchips." (Photo by John F. Cook)

Director's Message

The onslaught of VLSI technology has brought a vast new set of possibilities to compact, high-functionality, low-cost applications. Tens of millions of transistors can be fabricated on a single integrated circuit chip, but the design of these systems remains a huge challenge.

RLE's Circuits and Systems Group is developing new design methodologies and building novel chips to serve these increasingly aggressive applications. Techniques for logic synthesis, design for testability, high-accuracy circuit extraction, device and circuit simulation, highly parallel design architectures, consistent design frameworks, functional verification, and the realization of fast parallel systems are the main foci of this research. The common thread for these diverse projects is the need to characterize and optimize multiple views of a single design at several levels of abstraction, ranging from a high-level functional view to the geometrical mask specification needed for fabrication.

Many design techniques dwell at a single level of representation, but others provide transformations between these levels while maintaining their consistent relation. The need to break down the complexity of these large target systems is addressed through the techniques of structural partitioning, as well as the suppression of detail provided by the increased emphasis on higher level abstractions. Nevertheless, when performance is critical (and it usually is), there is no substitute for fine-grained manipulation of physically related models, and RLE's group has provided many algorithms aimed at the pursuit of high performance.

Professor Jonathan Allen, Director Research Laboratory of Electronics

The emerging trend of computer-aided design research is to provide the means to design (in all aspects) highly optimized, reliable systems that don't have to be iteratively fabricated to achieve design goals. As this research progresses, general techniques of design representation and evolution, optimization, and verification are becoming apparent. So, it will be no surprise to see this group provide new design methodologies for many other physical substrates, such as biological materials and micromechanical systems. Thus, design synthesis is becoming a generic discipline that will bring many technologies into highly useful systems.

VLSI COMPUTER-AIDED DESIGN

(continued)

aided design techniques, today's microchip designs would be impossible to create. This article is an overview of integrated circuit design and a look at RLE's research activities in this field.

Smaller and Smaller

Integration refers to the number of transistors placed on a single microchip. It reduces cost through economies of scale and improves circuit reliability at the chip level rather than at the circuit board level. Integration has mushroomed from small-scale integration (SSI) with about 4,000 transistors on chip, to very large-scale integration (VLSI), with hundreds of thousands of electronic devices on chip. In VLSI, the chip itself has become an integrated system containing approximately a million transistors and thousands of other components. VLSI systems have attained device dimensions smaller than the wavelength of visible light, and novel high-resolution lithographic techniques are used to fabricate these highly complex circuits (see ***currents,*** December 1988). Other rapidly emerging integration technologies include ULSIC (ultra-large-scale integrated circuit), which seeks to pack more than 4 million transistors on one chip with linewidths (the traces that conduct current) measuring 1 micron or less, and VHSIC (very high-speed integrated circuit), with a goal of tens of millions of transistors on a chip.

Tracing the Electronic Circuit

Electron or vacuum tubes were introduced in 1904 with Sir John Ambrose

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Fleming's invention of the diode tube, a "valve" that could control or rectify alternating current. Later that year, American inventor Lee DeForest discovered the triode tube, which not only controlled current flow, but also functioned as an electronic switch. In 1945, vacuum tubes were used in the first operational electronic computer, the ENIAC (Electronic Numerical Integrator and Calculator). It filled an entire room at the University of Pennsylvania, weighed 60,000 pounds, and used 18,000 vacuum tubes to perform computations. Unfortunately, because the vacuum tubes generated high temperatures (400° F) and consumed enormous amounts of energy, they needed to be constantly replaced.

The age of microelectronics arrived in 1947 with the invention of the transistor. Bell Telephone Laboratory physicists John Bardeen and Walter H. Brattain designed the point contact transistor using two wires positioned on a germanium crystal. Later that year, fellow Bell physicist William B. Shockley invented the junction or bipolar transistor. An improvement on the point contact transistor, the bipolar transistor had no wires to align and exploited the conducting properties of silicon, another semiconducting element less temperature-sensitive than germanium. Because only the charge carriers move in the semiconductor's crystal lattice, transistors became known as solid-state devices. An improvement over vacuum tubes, they consumed much less power, generated little heat, and could be bat-

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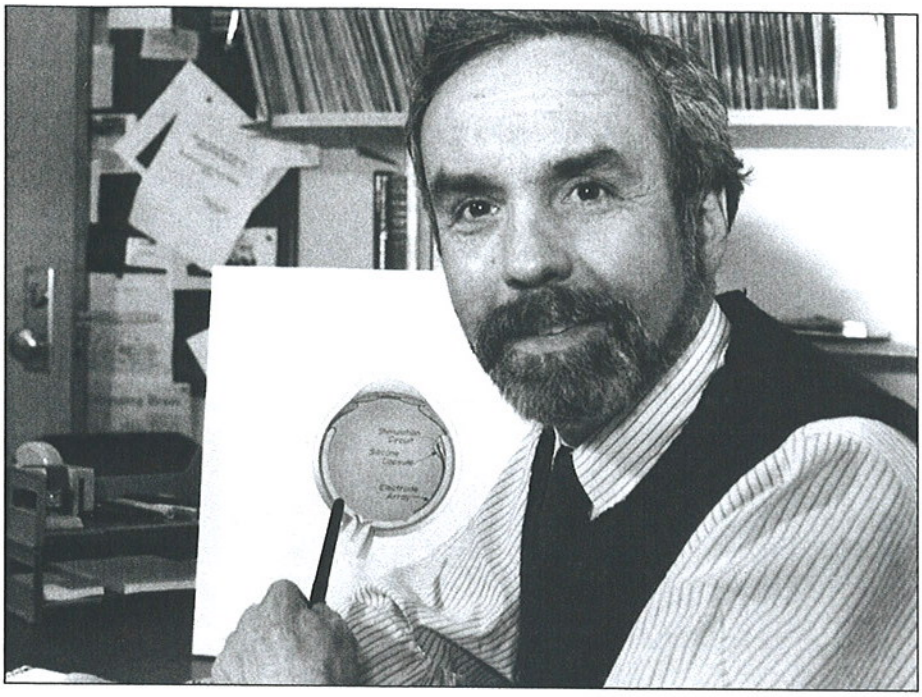
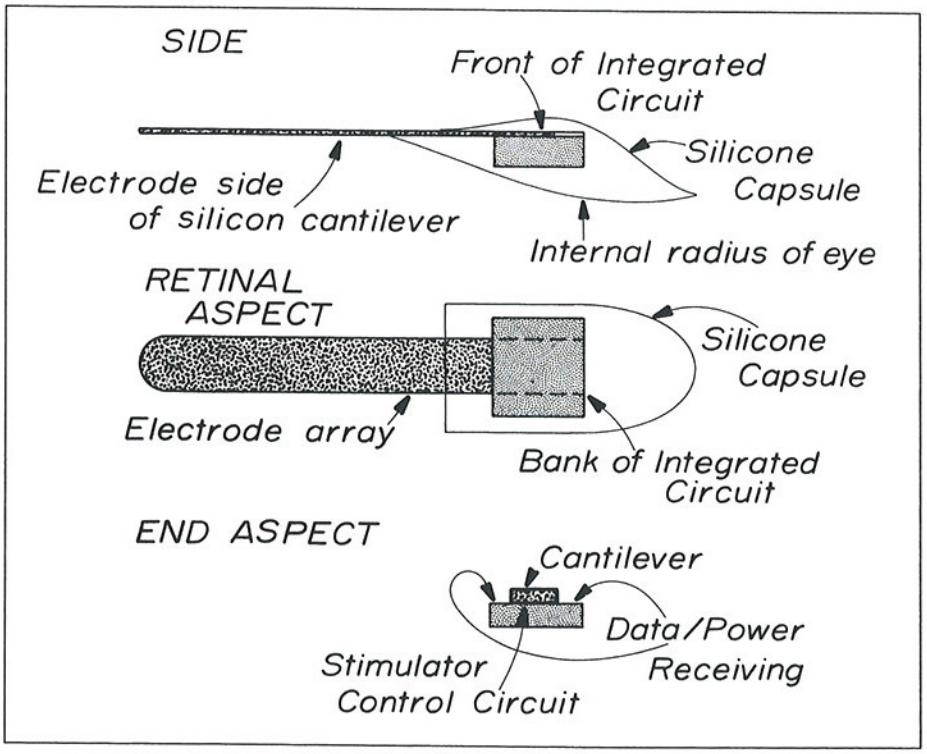
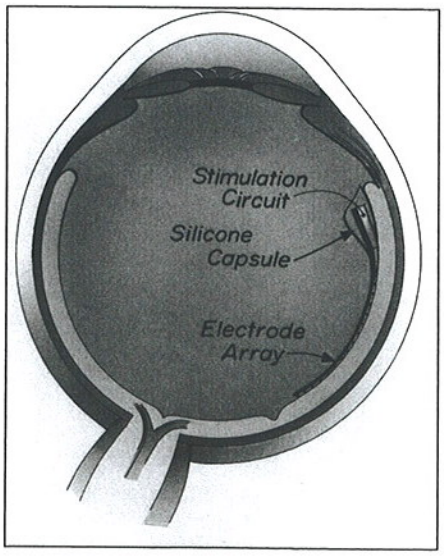


Professor John L. Wyatt, Jr. is part of a research team that is attempting to design an implantable silicon chip that will restore vision to patients with diseases of the outer retina. (Photo by John F. Cook)





An artist's rendition (above) of the implantable silicon retina microchip and its electrode array on the retinal surface currently being developed by Professor John L. Wyatt, Jr. and his collaborators. The chip will be surgically implanted adjacent to the retina. Light will pass through the lens of the eye and focus on the chip. Electrical pulses will then be transmitted to the retina through an on-chip array of stimulating electrodes. The pulses will directly stimulate the optic nerve or ganglion cells in the retina, causing them to fire as if they were stimulated by healthy photoreceptors. (At left) A cross section of the eye that shows the planned position of the chip as it is implanted adjacent to the retina.

tery powered. Transistors were first used commercially in Raytheon hearing aids and Texas Instruments portable radios. These discoveries earned Bardeen, Brattain, and Shockley the 1956 Nobel Prize in physics.

These first transistors had fragile wires that connected them to a circuit board, and were prone to breaking off. In 1957, attempting to fix this problem, scientists at Fairchild Semiconductor devised the first integrated circuit by placing all transistor components on and in a single layer of semiconductor material called a *substrate.* The first working integrated circuit (made of germanium) was announced by Jack Kilby of Texas Instruments in 1957. Later that year, Fairchild scientists designed a silicon integrated circuit using the *planar process,* where all circuit activity occurred on a few related planes in the integrated circuit, thus making it more efficient and easier to produce. The planar process became the standard for the manufacture of all integrated circuits.

In 1957, when the Soviet satellite Sputnik was launched, the space race began. The U.S. government invested heavily in the microelectronics industry, and the fierce competition between Americans and Soviets fueled the rapid pace of research. In 1959, a single chip contained only one device component, but by 1970 it contained 30,000 components. Microelectronics is a cornerstone in the American space program, and proved vital to its success during the '60s.

The "computer on a chip" was realized in 1971 with the invention of the microprocessor by Marcian "Ted" Hoff of Intel. It differed from earlier integrated circuits because it combined all computer operations on one microchip. In a space no larger than the head of a nail, the microprocessor incorporated a central processing unit (CPU), memory, controllers, buffers, input, and output. One microprocessor consumes $1/1{,}000{,}000$ the power and costs $1/30{,}000$ the price of the ENIAC, and it performs 200 times faster. Compared to other simple computer logic chips whose functions are hard-wired in an integrated circuit, a microprocessor's operations can be changed by simply altering its program. Microprocessors have opened the way for smaller, programmable appliances and equipment capable of robotics and precise measurements. Without them, personal computers and their smaller relatives would not be possible.

Elements of a System

Integrated circuits eliminated the many discrete electronic components that make up a hard-wired circuit (including resistors, inductors, and capacitors). Instead, semiconductor materials such as silicon and germanium now do the work of these individual components. Because they are smaller, more reliable, cost less, and perform better than conventional circuits, semiconductor integrated circuits are now the basic components of today's electronic systems.

Extremely pure silicon is used as a base semiconductor material for integrated circuits. By *doping* (combining) silicon with phosphorus, the silicon acquires excess electrons and is called *n-type* silicon. Doped with boron, the silicon has a lack of electrons and is called *p-type* silicon. When p-type and n-type are juxtaposed, electrons and holes (arising from the incomplete bonds) flow under the influence of an applied voltage. Since current can flow only from p-type to n-type material, it functions as a one-way switch called a *semiconductor diode* (similar to DeForest's earlier vacuum tube diode). The semiconductor diode is the foundation of the bipolar transistor used in high-speed computer applications. Here, a sandwich of n- and p-type materials is formed that acts as both a switch and an amplifier (similar to Shockley's earlier junction transistor). In order to perform logical functions, the silicon materials are combined on one surface (side by side or stacked) and etched into well-defined areas in the planar process. This method provides pathways along which the electrons move.

There are several classes of circuits, formed by a variety of fabrication techniques and used in many different applications. The two major classes are analog and digital circuits. Analog circuits react continuously to input, as in a temperature sensor. Conversely, digital circuits are two-state devices (on/off) and handle inputs in the form of binary digits or *bits* (0/1). Hybrid analog/digital chips contain both types of circuits; for example, an analog sensor whose data is converted to a digital read-out.

Gate circuits perform fundamental logic operations by selecting and transmitting part of the input signal while blocking out the rest (*e.g.*, one of every ten pulses). *Logic* circuits (including gate circuits, but not vice versa) are made by connecting two or more logic gates, and address only the presence or absence of signals, not their shape. By combining various logic functions, circuit designers can provide digital chips with different operations.

Circuit or chip designs can be standard, semi-custom, or custom. Standard chips use the manufacturer's design and are the least expensive to fabricate because of economies of scale. Semi-custom chips follow a standard design, but use two techniques to customize applications: by manipulating the logic function of the logic gates in the gate arrays and determining which gates will be connected or active, or by adding an extra layer of metal interconnect for more functions. Custom circuits follow a proprietary design and layout and are made for a highly specific application. Custom chips are costly and the most time consuming to design and manufacture.

Other major classes of semiconductor circuit include metal-oxide semiconductor field-effect transistors or MOSFETS. They are grouped by their fabrication process: complementary MOS (CMOS), p-type MOS (PMOS), and n-type MOS (NMOS). These circuits operate on low power and produce less heat than bipolar devices.

The Automated Approach to Microelectronic System Design

In automating the design process, there are several levels at which designers operate. The entire design process can be viewed as a sequence of transformations at and between various design levels. A structured design method builds in consistency between the *behavioral, structural,* and *physical* representations present at all levels in the process. This structured approach helps to simplify the design and reduce errors. One method of structured design is *abstraction,* where simplified models represent the actual objects and their functions. Abstraction helps to suppress detailed information and gives structure to a problem, thus making it easier to solve. In complex systems, several levels of hierarchical abstraction may be necessary to describe an object. Hierarchy helps to divide the circuit into multiple levels and reduce design complexity. Levels of abstraction in the design process include:

Functional design, where the designer determines the input and output behavior of major components in a system

and their role in solving a specific problem. At this level, the designer uses a high-level description language to develop a behavior representation (for example, a circuit's function) or the system's architecture.

System architecture, where individual functions of each system component are decomposed into blocks of various register subsystems to indicate parallelism. At this level, it must be determined whether or not the intended system can meet specific performance objectives, given the architecture and technology used. If not, alternatives must be explored.

Logic design, which defines the logic structure that will implement the functional design. Structural representations are either a textual or schematic description, and analysis is made by simulations at the gate or register levels.

Circuit design, where the designer addresses the currents and voltages that will operate in a system. By using components developed in the logic design phase, and keeping in mind the system's overall design, the designer builds the system's transistor circuits. Using automatic synthesis tools, the transistors are properly sized to meet signal delay requirements. Circuit and timing simulations analyze the design, and timing verification tools check signal delay specifications.

Physical design, where the designer determines how a system will actually be constructed. The behavioral and structural representations of earlier design stages are translated into geometric representations used to manufacture the system. Automatic synthesis, analysis, and verification tools are used to transform the earlier circuit design into a mask specification layout that is used in chip fabrication.

Other techniques in structured design include *regularity,* which reduces complexity through the use of iteration, and *standardization.*

Computer-Aided Design in VLSI

Interactive graphic workstations enable the user to create detailed visual information while communicating with a powerful, automated system. Computer-aided design (CAD) is used for geometric modeling, analysis, testing, drafting, and documentation. It is also applied to engineering (automated design, simulation analysis, process and tool design) and manufacturing (numerical control, robotics, processing planning, and factory management).

Because highly complex microprocessor designs have become too difficult to draft manually, circuit designers use computer-aided design methods to lay them out. Within the last 15 years, integrated circuit design has progressed from an entirely manual process to one that is substantially automated. Powerful CAD workstations perform many time-consuming, repetitive tasks while permitting designers and engineers to focus on analysis and creativity. A CAD workstation can display all or part of a circuit diagram to verify a correct design, change the function of a logic device, calculate how a microprocessor will work while its design is in progress, and store room-sized diagrams.

CAD software tools assist the development of techniques and algorithms. There are currently four types of CAD tools that support the physical design of an integrated circuit. The first is the *geometric* approach, where a commercially available interactive graphic system is used by the designer to create the exact shape of a structure on an integrated circuit mask. In the *symbolic* approach, details are hidden and the designer works with symbols that the CAD system converts to exact geometries. In the *cell-based* approach, individual function cells and performance data can be completely characterized and their specifications stored in a computerized cell library. As the library grows, the building of block diagrams and their subsequent conversion into mask layouts for chip fabrication becomes more efficient. Finally, in the *procedural* method, cells are automatically placed in a complete integrated circuit layout that uses a procedural language to describe their placement and interconnections. The trend in CAD tools has been towards *delayed binding.* This means deferring decisions on a circuit's components and functions as late as possible in the design to afford the designer more flexibility in the process.

CAD tests a circuit design by simulating it, rather than constructing expensive breadboarding or hardware. Previously, in hardware testing, costly errors often did not appear until the chip was already fabricated. Through the use of CAD, a circuit's timing can be tested separately from its logic functions, and corrections can be made less expensively at the design stage.

Levels of Representation in the Design Process

Throughout the integrated circuit design process, several different views or representations show various aspects of the system. These are the behavioral, structural, and physical representations.

Behavioral Specification

At the beginning of the design process, the designer develops a behavioral description of a circuit's function and determines which algorithms will be coded to perform this particular function. The behavioral description is then simulated by compiling and executing a functional language program or by using a behavioral simulator with its own language.

Once simulated, the behavioral description is translated into a structural or circuit description. Structural representations, such as block diagrams and schematic drawings, show the composition of circuit elements in terms of components and their interconnections. In its simplest form, a structural description is a *net list,* which represents the interconnections of cells and logic gates in a design. The net list shows topological connections but not the geometry of cell locations on a chip.

High-Level Synthesis

High-level or system-level synthesis involves the *partitioning* or specification of various subsystems. This "divide and conquer" approach helps to manage complexity and imposes more structure on a design. It is usually done manually for designs that do not require any design exploration. Partitioning is associated with the development of a system concept and the definition of a realizable architecture and its requirements.

Architectural exploration is performed during high-level synthesis and involves the mapping of variables to registers or signals, operators to functional units, and control structures to controller operations. The goal of architectural exploration is to find the optimal implementation of a circuit. It entails a heuristic or exhaustive search of the design space to explore the different ways in which the design can be implemented.

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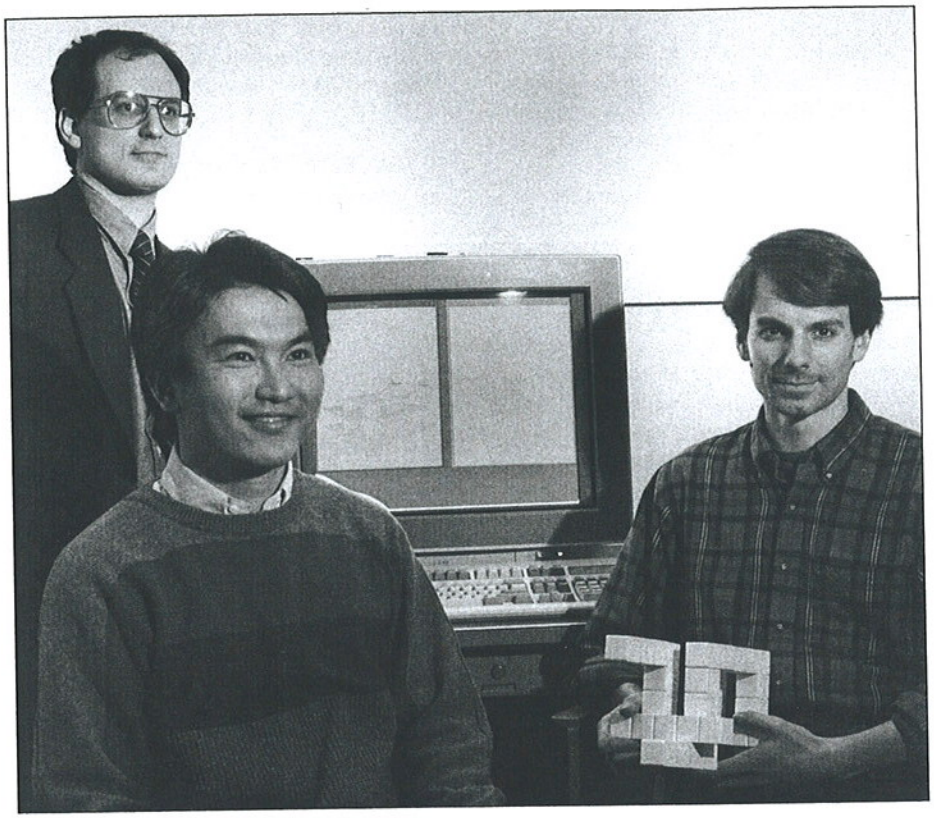
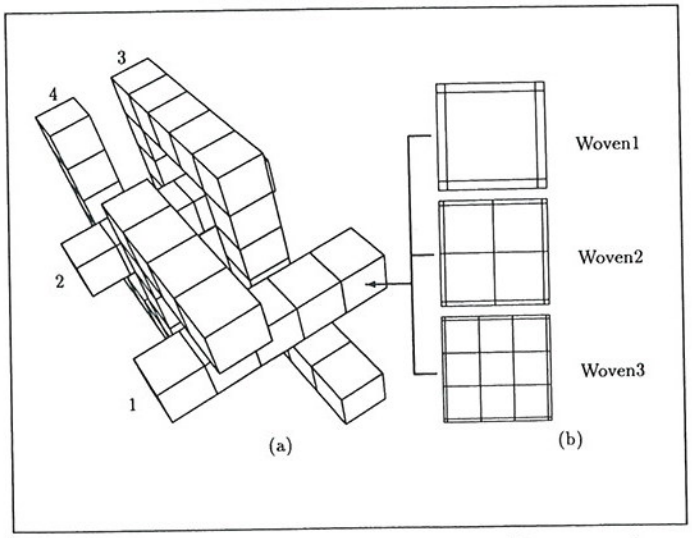


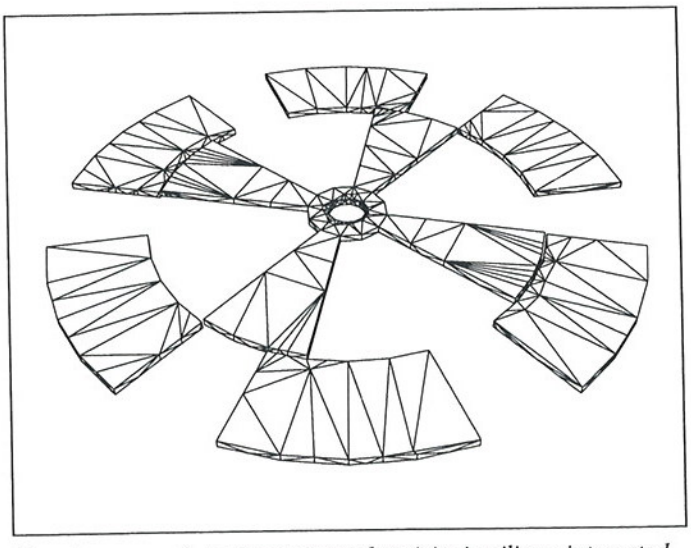
Professor Jacob K. White and graduate students Songmin Kim and Keith S. Nabors demonstrate the types of three-dimensional integrated circuit and packaging structures that can be routinely analyzed by FASTCAP, a very fast capacitance extraction program developed at MIT. Using a computer-aided design workstation, FASTCAP can quickly and accurately analyze complex structures. It uses a novel multipole-accelerated, preconditioned iterative method to compute surface charge densities. FASTCAP's capabilities are being extended to perform three-dimensional inductance extraction and transient interconnect analysis. (Photo by John F. Cook)

Tasks include: *resource allocation*, the selection of the type and number of functional units; *scheduling*, the assignment of time slots to the components' operations; and *resource assignment*, the assignment of operations to specifiic functional components. The allocation of more resources results in a more parallel system with greater performance, but with a higher hardware cost and larger chip area. This is known as a trade-off between time and area. System-level synthesis produces a description of the data path and controllers.

The next step is *register transfer-level synthesis*, where a functional or register transfer-level model describes the implementation of the data path and controller. Data path optimization is aimed at better resource allocation and assignment for both timing and area. Tasks in data path optimization include *resynthesis* for a variety of block implementations and *register relocation* to achieve structural modifications. The controller, which generates control variables for registers and memory units, is transformed from its abstract description to a *finite-state system*. In this transformation, controller architecture is selected, states are assigned, inputs and outputs are encoded, and the controller



An illustration of a woven bus interconnect problem in an integrated circuit that was solved by Professor Jacob White and his students using the FASTCAP program. Successively finer panelings of a bus' surface are shown in (b), which represent a set of nested discretizations used to perform numerical simulation. The FASTCAP program, developed at MIT, can compute the surface charge densities on these structures and can solve problems involving the discretizations of thousands of panels in only a few minutes on a scientific workstation.



Growing research and commercial activity in silicon integrated circuit-based micromechanical structures has piqued interest in computer-aided design tools for this field. At RLE, Professor Jacob K. White and his collaborators are developing a MicroElectro-Mechanical Computer-Aided Design system (MEMCAD) to assist designers in performing realistic simulations for structures such as microsensors and micromotors. The MEMCAD system was used to perform electrostatic force analysis on this solid model of a micromotor.

is decomposed into smaller, interacting finite-state machines (sequential circuits with a finite number of possible states). Register transfer-level synthesis produces a system that is decomposed into blocks of *combinational logic*, where outputs are entirely dependent upon inputs, and *sequential storage components*, where inputs plus the state of memory elements in the circuit determine the outputs.

Results from the register transfer-level synthesis are optimized and mapped to a gate-level hardware structure or a schematic in logic-level synthesis, where the system is described as an interconnection of switching elements or gates. At this level, the goal is to minimize logic in both path delay and area, and to ensure the logical correctness of the design to implement the various blocks. If the system utilizes a two-level logic architecture, the results are sent to a PLA generator. If the architecture uses multi-level logic, then *technology mapping* is used.

Technology mapping uses the network of technology-independent abstract logic gates developed in logical-level synthesis and maps them to elements of a specific semi-custom cell library. Thus, technology data is added to the earlier structural description and results in an abstract hardware network. The different methods of technology mapping produce a variety of area and delay values. Issues involved in technology mapping include whether or not it should be the first or last synthesis design step, and which technology should be selected. As synthesis moves to higher levels of abstraction, technology mapping moves into the earlier stages of design. It is important that the mapping of an abstract, technology-independent circuit to a specific target architecture meet *testability* requirements. These requirements are related to *design for testability*, where the goals are controllability (control of circuit nodes so they can be tested) and observability (the ability to observe faults).

Physical Design

The physical design stage transforms circuit design specifications into physical mask representations used to manufacture the electronic circuit. The designer must follow strict geometric design rules associated with the constraints of the fabrication process. These include requirements for minimum feature sizes of the various components, as well as the spacings and connections between them. Failure to follow these rules can make the chip inoperable, unreliable, or unmanufacturable.

Today's computer-aided design methods speed the process of physical design by automatically translating specifications from the chip's behavioral or structural description to its physical layout. The designer uses automatic layout techniques to quickly map the structural representation into a circuit's physical representation. Although these techniques result in a more error-free layout, the layout itself may not be as efficient or creative as one produced by a human designer. The designer must also be concerned with both the placement of components and their interconnections.

This phase of design begins with a physical representation or floorplan that consists of geometric coordinates for the circuit elements and interconnection. The designer uses the floorplan to determine actual structures as they relate to the circuit's logic functions, to estimate the size and position of major blocks in the system, and to check timing paths. From this floorplan, a symbolic layout with predefined cells is constructed.

A *mask layout* is generated from this symbolic layout and consists of two-dimensional patterns (rectangles) to represent the different mask patterns used in circuit fabrication. A *layout editor* is used to draw the graphical shapes that define the mask layout. The editor does not check these shapes, so testing must be done to ensure their correctness. Symbolic layout editors can be used to limit the shapes available to the designer, thus minimizing layout errors, but at a cost trade-off in layout density.

In the procedural or program-driven synthesis method, computer programming techniques such as conditionals, loops, variables, and procedure calls are used to create graphical objects. Compactors (or compaction algorithms) can also be used to automate a circuit's geometric design by moving its components and wires to optimize space.

During the synthesis phase of physical design, tools for *automatic placement* (to position components on a layout surface) and *routing* (to interconnect components with wiring) create new or improved layouts from earlier structural representations. These include:

A placer, which maps the cells to predefined physical gates. By optimizing details from a net list description, such as the total length of wire used to connect the cells, it assigns those gates to locations on the chip.

Various *routing algorithms* that can be chosen to generate the wires connecting the cells. Channel routers simultaneously route all wires in rectangular areas. A maze router routes wires individually on a grid, taking into account barriers or blockages.

A *programmable logic array* (PLA) produced by a PLA generator program. From a set of Boolean functions, arbitrary two-level logic is transformed into a geometric structure. A logic or PLA optimizer minimizes the logic in a PLA to reduce its area without changing its function.

A *silicon compiler* that builds a physical description or layout of a chip from its behavioral description. The designer specifies a design structure, then the circuit's parameters (functional, electrical, and geometrical) are processed by corresponding module compilers. All relevant design rules are stored in a *technology file* to check the circuit. Timing and logic models are also generated for each component in the circuit. The system then uses placement and routing or PLAs to form a chip composite. A package editor supplies packaging information for the fabrication process, and a simulator can then test the chip.

Simulation

Simulation ensures that the chosen design is the one needed to perform all the desired functions. It also determines the circuit's operating speed and checks any delays or faults that might be present. The determination of accurate circuit timing during simulation is a trade-off in terms of determining the optimal performance of the circuit. Computer-aided design tools can be used to simulate performance at all levels of representation. A variety of simulators for behavior, logic, and transistor switch-level timing include *gate-level* or *logic simulators* for logic gates, *transistor* or *switch simulators,* and highly accurate *circuit simulators. Timing simulators* are gate-level or transistor simulators for accurate timing. *Mixed-mode simulators* allow a combination of simulation

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modes. A *timing analyzer* can be used to estimate path delays without simulation.

Analysis, Verification, and Testing

Analysis, verification, and concern for testing procedures are found within all levels of design—from a system's behavioral specification through its physical design.

Analysis

Because fabrication of an integrated circuit is time consuming and expensive, chip analysis and verification is essential before it is manufactured. Analysis operations evaluate the consistency or correctness of a chip's behavioral, structural, and physical design representations. A variety of tools are used to check errors:

The automated *design rule checker* (DRC) is a reliable method used to check layout geometry to ensure that it follows the design rules.

Circuit extractors analyze the layout, then extract a net list of transistors, thus converting a physical description back to a structural description. The structural circuit description can then be simulated with a switch or circuit simulator. Programs to verify the extracted net list include: a *network comparison program,* which compares the net list from the circuit design phase to the extracted net list from physical design; and an *electrical rules checker* (ERC), which checks the electrical properties of a circuit. *Parameter extractors* can determine electrical parameters from layout information for timing simulation.

Verification

Verification is the final phase of design. It is a formal process to demonstrate the equivalence of two design representations under all specified conditions. One example is to compare a schematic diagram and a physical layout that has been synthesized from that schematic. In many cases, formal verification techniques are preferred over simulation because it results in a reliable mathematical proof rather than the experimental results of test case simulation.

Testing

Testing has come to the forefront in VLSI, whereas in previous years it was considered a secondary concern to the overall design process. Testing involves checking the completed integrated circuit to see if it was manufactured correctly and to determine if the final design is the one that the designer had intended to build. Testing simulates operating conditions and detects faults at the circuit level which may affect performance. A set of *test vectors* are developed in a test language to detect a circuit's input and output behavior. *Test generators* can automatically develop a set of tests for a particular circuit, although they require some restrictions on the design. *Fault simulators* grade tests by simulating a circuit, assuming a fault, and verifying that the test vectors propagate the differences as a result of that fault as seen in the outputs. The most common fault model found in integrated circuits are *stuck-at faults,* where a node is stuck in the on or off position. The percentage of faults detected indicates the quality of the test. Testing indicates the *yield,* or number of functioning chips, and the test engineer may recommend design improvements to correct the observed defects.

VLSI Computer-Aided Design in RLE

RLE research activities in VLSI technology range from crystal growth for semiconductor materials to new photolithographic fabrication processes. Additional research involves device physics and the design of computational algorithms. The ongoing investigations in RLE's Circuits and Systems Group seek to provide the means for designing custom integrated circuits quickly, correctly, and economically.

Professor Jonathan Allen's research is concerned with performance-directed synthesis of VLSI systems. He and his students explore the development of new CAD tools that can serve as an integrated framework for design exploration while providing high-performance circuit optimization and consistently aligned representations at all levels of the design process.

A current project focuses on basic methodologies for very high-speed clocking strategies. Using CMOS technology, a new circuit style called *true single-phase clocking* enables clock speeds of several hundred megahertz. The cause for this high-speed performance is now under study. The circuit is expected to be used in a wide variety of applications and provide an important capability to performance-directed synthesis. Further studies also seek to provide a systematic design methodology for this new class of circuits.

Another system under study will permit comprehensive architectural design exploration while predicting the speed performance of a proposed design. This work involves the systematic exploration of signal processing algorithms and architectural alternatives, then extending the results to the layout level. The project has already contributed highly optimized array architectures for digital signal processing systems.

An innovative VLSI design database is being developed that will supply automatic consistency maintenance between several design representations. The goal of this work is a database design that will automatically, incrementally, and continuously provide for consistent alignment of all levels of design abstraction. The project is now being extended to include other design modules, the introduction of new schema compilers, and the extension of its basic methodology to functional representations.

Other important research in Professor Allen's group concerns the development of new techniques to concisely represent waveform transition effects in integrated circuits. These techniques were combined with macromodeling techniques to accurately characterize integrated circuit systems. Also, grammatical techniques that verify the correctness of circuit style were extended to semantic tests that check for device size, charge sharing, and other electrical phenomena not easily represented in grammatical form.

Professor John L. Wyatt, Jr. and his collaborators are building VLSI chips for machine vision, and have produced three camera processor chips that operate at over 1,000 frames per second. The goal of this research, known as the MIT Vision Chip Project, is to design and build a very powerful, fast, and compact early vision system that can operate in real time.

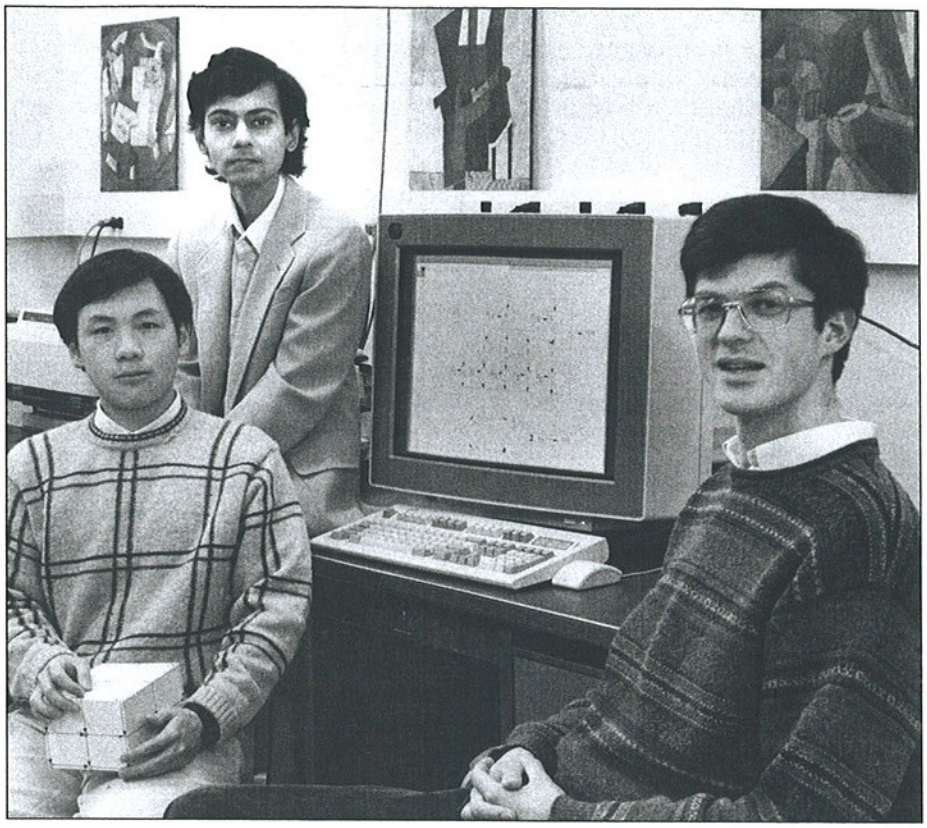
Early vision refers to a set of processes that recover the physical properties of three-dimensional objects from a two-dimensional array of image intensity data. Early vision systems process raw visual data such as the fine details of texture and spatial gradients or temporal changes in incident light intensity. The

system produces a simplified representation of an image in which features such as boundaries and information on depth and velocity have been extracted. Its results are passed to a higher level system that can perform object recognition, scene analysis, or robot navigation.

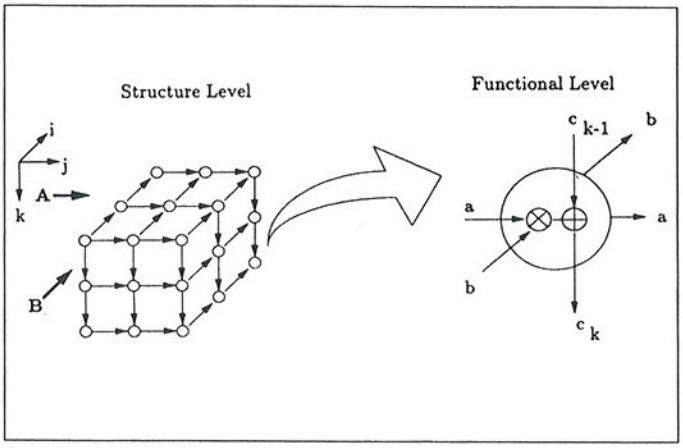
Investigators chose to design an analog early vision system because it is simpler, faster, and uses less space than digital circuitry. Tasks involve hardware development for existing algorithms and modifying other algorithms to match the hardware's specific requirements. The project has brought together several investigators with a broad range of expertise in CMOS and charge coupled device (CCD) technology, innovative circuit and system design, robotic algorithms, physiology, nonlinear circuit theory, parallel computation, and fabrication technology. Many of the system's chips are custom made and require custom fabrication at MIT's Microsystems Technology Laboratories.

In a highly experimental project, Professor Wyatt is also part of a second team that is attempting to design and construct a silicon retinal implant chip for the blind. The retina is a delicate and complex tissue (it is considered part of

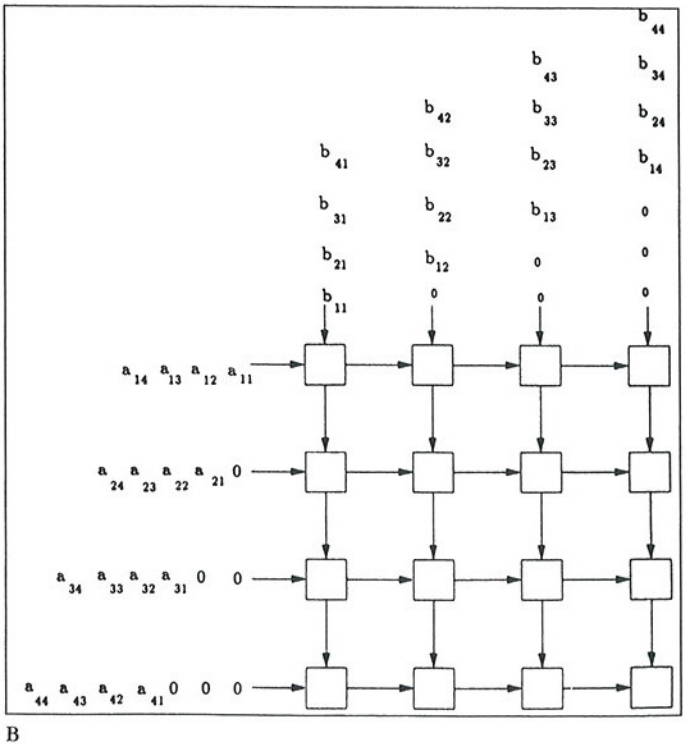
(continued on page 10)



In an abstract cubist environment, Professor Srinivas Devadas (center) and graduate students Stan Y. Liao (left) and Filip J. Van Aelten study verification procedures to ensure digital circuit designs are consistent with signal flow graphs. A signal flow graph is an abstract representation of a specific computation that is to be performed. Stan holds a model cube that illustrates a typical signal flow graph to which array-based processors must conform. The computer monitor displays a signal flow graph and the microcoded processor that implements it. (Photo by John F. Cook)



A



B

These figures illustrate a simple specification/implementation pair for matrix multiplication used by Professor Srinivas Devadas and his students. The specification (A) is a three-dimensional signal flow graph where every node performs a multiplication and an addition. Deriving an implementation from this specification involves the tasks of hardware allocation and scheduling. The resulting implementation (B) is a two-dimensional array processor. The verification task is to check if the input/output behaviors of both the specification and the implementation are in a certain formal relation.

the brain), and vision loss is usually permanent. Some patients can be helped with special low-vision glasses, but there is currently no medical treatment available to repair retinal damage. The team (which includes investigators from the Massachusetts Eye and Ear Infirmary, Massachusetts General Hospital, Lincoln Laboratory, and RLE) is designing a prosthesis that may help restore vision to these patients, especially those suffering from macular degeneration and retinitis pigmentosa.

The prosthesis will be a two-sided silicon microchip implanted adjacent to the retina. Light passing through the eye's lens will be focused on a photoreceptor array located on the chip, and electrical impulses will be sent to the retina through an array of stimulating electrodes also on the chip. Healthy optic nerve cells in the retina will be stimulated by the pulses, causing them to fire. Because this research is in its early stages, there are still many issues to be addressed, such as how to design and mount the device properly so there is no discomfort or further damage to the retina, yet close enough to ensure sufficient electrical stimulation. Questions also must be answered about the toxicity of the device and the effects of electrical stimulation on the retina.

Professor Jacob K. White and his students perform numerical analysis for circuit and device simulation. They also investigate parallel computation and the interactions between numerical algorithms and computer architecture.

His group's research has contributed to circuit and device simulation using *waveform relaxation* techniques. Waveform relaxation is an iterative method used to analyze nonlinear dynamical systems in the time domain. At each iteration, the method decomposes the system into several dynamical subsystems. Each subsystem is analyzed for the entire given time interval. The efficiency of these methods has been improved for circuit simulation and, recently, the techniques were accelerated to reduce relaxation iterations by almost an order of magnitude. These algorithms may be effective in solving a broad range of time-dependent partial differential equations, such as those in fluid mechanics, and may lead to very efficient parallel simulation algorithms.

Another project addresses simulation algorithms for clocked analog circuits, where frequency and time-domain techniques are combined to analyze switching circuits. Algorithms have been developed to simulate switched capacitor filters and switching power converters. These methods are based on accurately simulating selected cycles of a high-frequency clock with a standard discretization method and then combining the selected cycles by computing the low-frequency behavior with either a truncated Fourier series for steady-state calculations or low-order polynomials for transient calculations. By accurately computing the solution over a few selected cycles, an accurate long-time solution can be attained. This is known as an *envelope-following algorithm.*

Approaches to more accurately compute the electric fields in MOS devices are also being explored. Numerical techniques to solve the energy balance equation for electron temperatures were proven and used to predict substrate currents in MOS devices. A method was derived that uses a two-dimensional simulator developed by the group. The predicted results matched the measured data on devices with channel lengths as short as 0.16 micron. Monte Carlo techniques are also being evaluated for device simulation on massively parallel computers. Monte Carlo simulation methods approximate the behavior of a system by performing a single computation many times using a random-number input, then examining the statistical distribution of the results to help make a design decision. Monte Carlo methods are used when a problem is too complex for a closed-form mathematical solution. These techniques are now being used in transient calculations with self-consistent electric fields.

A program has been devised to provide three-dimensional capacitance extraction in linear time. It is based on a novel adaptive multipole algorithm that is three orders of magnitude faster than standard techniques. The program, FASTCAP, has been generalized to cover a broad class of applications including the computation of torque by micromotor designers. Recent improvements to FASTCAP have resulted in performance faster than standard boundary-element-based programs and have achieved more accurate results for complex problems while retaining the linear time complexity of the basic algorithm.

The group is also taking an applications-oriented approach to parallel numerical algorithms in circuit and device simulation. Application programs and techniques are being developed for both massively parallel single and multiple instruction, multiple data machines. In addition, they are seeking to understand the fundamental aspects of the interaction between architecture and certain numerical algorithms.

Also underway is a project to develop a microelectromechanical CAD system that will enable microsensor designers to easily perform realistic simulations. The system currently performs electromechanical analyses; for example, calculating capacitance versus pressure for a square diaphragm deformed by differential pressure.

Professor White has used his numerical analysis techniques to assist other RLE investigators. In the Auditory Physiology Group, two-dimensional steady-state fluid calculations were carried out for cochlear hydrodynamics. In the Electromagnetics Group, these techniques helped to solve inductance calculations and problems involving transmission lines with nonlinear loads. Simlab, an interactive and easily modified circuit simulator, was developed for the MIT Vision Chip Project. It is used to investigate simulation techniques for circuits in early vision research.

Professor Srinivas Devadas and his group explore all aspects of computer-aided design for integrated circuits and systems, including the development of new techniques to perform automated logic synthesis, design verification, and VLSI system testing. He and his students devise logic optimization methods that consider not only area, performance, and power consumption, but also the testability of a designed circuit. The group also develops verification methods for the behavioral, logic, and circuit levels, and devises efficient test generation methods at the logic level that can easily test fabricated integrated circuits. This research involves developing new algorithms, proving theoretical results from these algorithms, and demonstrating their effectiveness by creating software programs that solve practical problems.

Professor Devadas and his students have developed a method to precisely and efficiently compute logic circuit delay using timed test generation. They are also working on an analysis of statistical delay to accurately predict the percentage of fabricated integrated circuit chips

that will meet a desired performance goal. The group has also formulated a calculus of event simulation and has applied it to different models of timing behavior so the number of events that need to be evaluated in a circuit simulation can be reduced. Using conventional stuck-at-fault testing techniques, they have developed a unique delay computation algorithm for all functioning circuit delay paths.

Another project employs string function theory to develop an efficient and formal methodology that will verify logic implementations when compared to behavioral specification. New definitions of behavioral equivalence (for example, equivalence relations between serial, parallel, and pipelined implementations of behavioral specifications) were established that use this string function theory. This research may produce a string function theory and formalism for behavioral synthesis.

The group studies new approaches to determine encoding problems associated with state assignment and finite-state machine decomposition. The goal of this research is to obtain logic-level implementations that are minimal in area and delay. The prime-factorization-based encoding of N-state counters has proven to be a successful approach. Decomposition-based methods have been used for state assignment to solve the encoding problem in general finite-state machines. The group also investigates the use of re-encoding techniques for sequential circuit optimization.

Professor Devadas and his collaborators have furthered the concept of VLSI synthesis and testing for testability. Theoretically, this approach has resulted in rigorous and formal characterizations of logic circuits. It has also provided methods for automatic synthesis to enable the design of VLSI circuits with unprecedented levels of testability (guaranteed 100% testability for delay faults; a fault model more comprehensive than customary stuck-at fault models). This research focuses on test generation under stuck-at and delay fault models for non-scan VLSI circuits, and synthesis for sequential testability.

Professor Devadas has developed several algorithms for fundamental logic synthesis problems and efficient formal verification methods. His work has resulted in a prototype system for CAD algorithms. One technique has led to the synthesis of a large speech recognition chip that is possibly the most testable circuit ever automatically synthesized and designed. The circuit contains approximately 25,000 transistors and is fully testable under the most comprehensive fault model currently known, the robust path delay model.

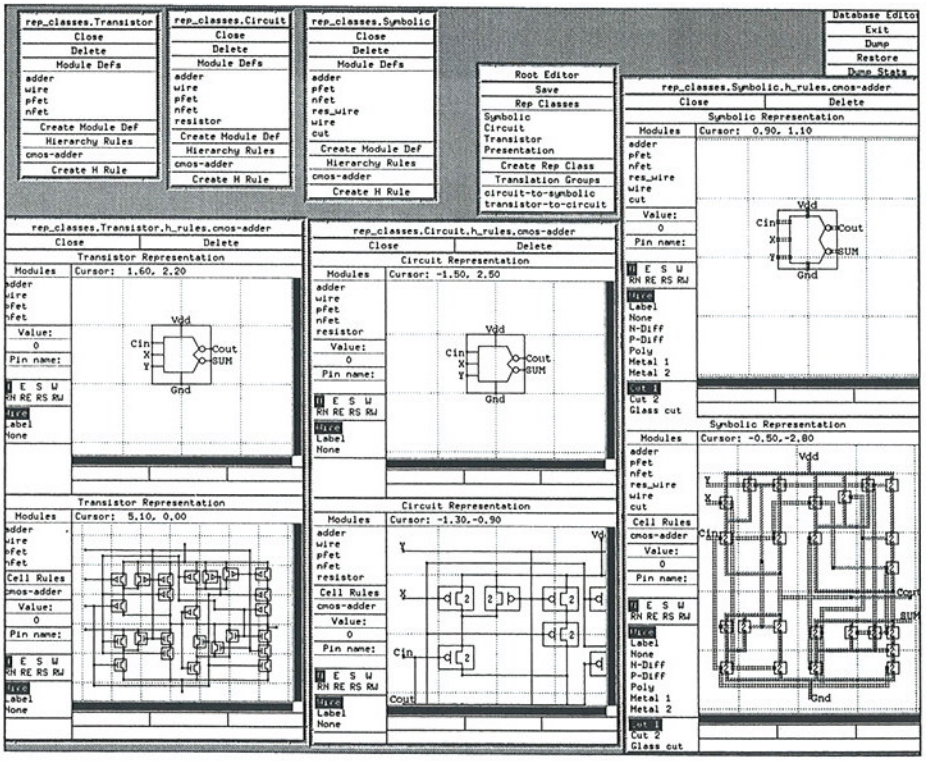
Other research activities in his group include the automated synthesis of circuits for low-power consumption and the development of built-in self-test techniques for the random pattern testability of a circuit design.

Future Directions in VLSI

It may one day be possible to automatically design reliable and economical VLSI systems from the algorithmic level through the fabrication of a circuit. To realize this potential, advances in CAD tools for VLSI must keep pace with the capabilities of fabrication technology.

The development of highly advanced CAD tools will not only result in high-performance computers and electronic devices, but the methods used to implement these tools may also be extended to a wide range of other disciplines such as computational biology, biochemistry, and artificial intelligence. An example is the current problem of matching DNA strings in biochemistry. This is a difficult, discrete combinatorial optimization problem that is also found in integrated circuit computer-aided design.

by Dorothy A. Fleischer



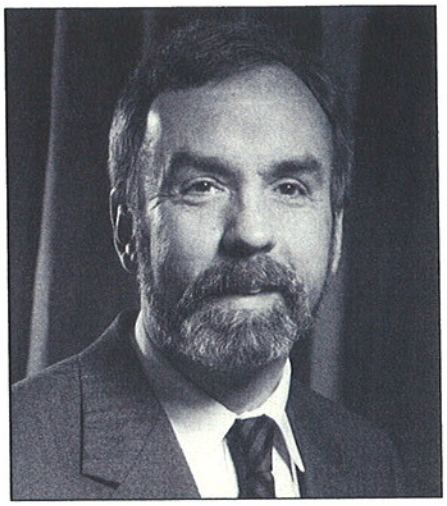
A prototype database manager used to design full-custom VLSI systems was recently developed by graduate student Robert C. Armstrong in Professor Jonathan Allen's group. The database manager, called FICOM (Framework for Incremental Consistency Maintenance), simultaneously displays the various design views of an integrated circuit (including its architectural form, logic diagram, circuit schematic, and mask layout geometry) and helps to maintain a consistent relation of all the views so that they correspond to the same circuit implementation. In this example, FICOM is used to design a full adder module. The three levels of abstraction are shown from left to right (transistor view, circuit schematic, and symbolic layout). The top row shows the module block views and the bottom row shows the module contents. FICOM vertically displays the circuit's structural hierarchy, while consistent views are displayed horizontally in an interrelated fashion. Changes made by the designer in one view are automatically translated to changes in other related views. This retains the overall consistency and well-formedness of a circuit's design.

FACULTY PROFILE:
John L. Wyatt, Jr.

You would be correct to say that Professor John L. Wyatt, Jr. is a man of vision. Currently, he is a member of two interdisciplinary research teams, the MIT Vision Chip Project which is exploring early vision, and another collaboration developing the design of an implantable retina microchip.

Professor Wyatt was born in Memphis, Tennessee, in 1946. He attended MIT (BSEE '68), Princeton University (MSEE '70), and the University of California/Berkeley (PhD '79). His early professional experience included stints as a design engineer with the U.S. Public Health Service from 1969 to 1971, and as a postdoctoral associate with the Medical College of Virginia from 1978 to 1979. Following his postdoctoral research, Professor Wyatt returned to MIT in 1979 as an assistant professor in the Electrical Engineering and Computer Science Department, and joined RLE's Communication Biophysics Group. He was promoted to associate professor in 1984, and to full professor in 1990. MIT's Department of Electrical Engineering and Computer Science named him the first Adler Scholar in 1990. The scholarship enabled Professor Wyatt to relinquish his teaching responsibilities for one semester to take a class in machine vision.

Professor Wyatt's broad range of knowledge encompasses areas of mathematics, engineering, neurophysiology, thermodynamics, biochemical transport, and VLSI design and simulation. His current research activities in RLE's Circuits and Systems Group focus on the dynamics of nonlinear circuits and systems, machine vision algorithms and analog VLSI for machine vision, and retinal stimulation using a microchip.



Professor John L. Wyatt, Jr. (Photo by John F. Cook)

• ***What sparked your interest in science and engineering?***

Originally, I started out as a junior chemist at age five. My childhood love was explosives. I made homemade gunpowder with a coffee grinder, which is great for grinding charcoal very fine, and made brightly colored bombs. The druggist around the corner gladly sold me potassium nitrate and flowers of sulfur, and I quickly branched out into many other kinds of explosives—zinc dust and sulfur, potassium perchlorate and sugar. I terrified my parents. Once, when I wasn't able to go to school, the kids asked, "Where's Jack, did he blow himself up?"

In grade school and junior high, I transmitted illegally on television frequencies and messed up all the televisions in the neighborhood. By the time I was in seventh grade, I was making homemade radios, even though I didn't understand them very well. I had a 250-foot antenna stretched from one backyard to another and picked up the Voice of the Andes from Quito, Ecuador. I never did get a ham license because I got bored learning Morse code.

During summers in high school, I attended classes at an industrially oriented high school taught by an excellent teacher, Hugh Phillips. He had a plaque that read "Father of Nicaraguan Radio." Apparently, he had put together their radio system. He taught high school kids who were interested in vacuum tube analysis and design to get their commercial radio engineers' license. In his class, we didn't learn mathematical theory because we hadn't learned calculus yet, but we did learn to design conventional circuits. Our final exam at the end of the second summer had no written material except a parts catalog. We were to build a five-tube superheterodyne AM receiver with whatever we wanted from the catalog. By the end of the class, we didn't just know about circuits, we had acquired the competence to build them ourselves. I was lucky to take the class because it helped determine my direction. I found my interest in electronics to be more compelling than my formal liberal arts education. The classes at my private school only taught me to do what many other people could do, whereas the technical high school prepared me to do things for my future, and I could do them myself.

• ***You had a good idea of where you were going quite early on.***

In high school, my ambition was to go to Italy, get a job until I learned the language, and join the Ferrari mechanics program. I had raced go-carts in National Carting Association races with friends, and I was a good two-cycle engine mechanic. College seemed too boring and conformist. I wanted to become a good race mechanic, and Ferrari seemed like the place to go. So, I didn't apply to college, but my dad applied for me. He told me that I could be a perfectly good Ferrari race mechanic with an MIT degree, that it wouldn't hinder me at all.

It didn't matter too much to me when I was accepted to MIT, but it was sheer excitement when I moved to Boston. It took away the last vestiges of juvenile delinquency. People here didn't tell me how I had to be, that I had to be like them, or that I had to see it their way. They had a lot to teach and they were going to tell me how it all worked. People at MIT complain that this place is not a hand-holding, protective community. There may be some validity to that, but I found it liberating. If it had been very protective, I would never have felt that I was on my own. It was an intellectually sharp community, and how I handled my life was entirely up to me. I wanted the intellectual wizards to guide me and say here it is; people like Art Mattuck in math and Tony French in physics. But,

after two years at MIT, despite all its wonder, I was burned out. I took my junior year in Germany, learned the language, went skiing, and studied comparative literature and philosophy. That gave me a wonderful junior year and brought me back to MIT rejuvenated.

• What happened after MIT?

I wanted to do a second bachelor's in math, but the draft board said no. I was attending graduate school at Princeton in electrical engineering and I was given time to complete my spring semester in 1969. I filed as a conscientious objector who was willing to take care of the wounded. That meant they would have sent me to Vietnam where I would have gone into combat without a gun. I didn't think of the practical consequences of my decision; I just checked off that particular box on my draft form because that's how I felt ethically. The U.S. has five armed services and two other uniformed services that are not armed—the Public Health Service and the Coast and Geodetic Survey. I was lucky to get a job at the Public Health Service in Maryland.

My two years there yielded my first patent. It was for a cheap, reliable radiation measurement instrument. I was able to devote full time to a real design project, and it reaffirmed my love for circuits. The instrument I designed used discrete components and was supposed to work down to one femtoampere (10^{-15} amperes). Unfortunately, it made a great seismograph. It would go off scale when trucks came down the highway over a quarter-mile away. I could stand across the lab, make a sharp move with my hands in the air, and drive it off scale. It was the most sensitive, if least accurate, seismograph I'd ever seen. The instrument worked this way for about a month, and then it hit me. I had built everything on high-quality ceramic standoff insulators so there would be no current leakage. I recalled something that I had read in the *Boys' First Book of Electricity* in the third grade—ceramics are piezoelectric! I had forgotten it and no one around there knew. The ceramics generated electricity every time there was the smallest movement. So, I put everything on Teflon insulators and the problems went away. It made me think that circuits were wonderful and magical, and it made me feel competent to be able to solve problems with them.

Eventually, the instrument was developed further and we applied for a patent on the whole system. It is widely used in Europe for low-level x-ray emission monitoring. Of course, I signed away my royalty rights to the government. In a way, it was nice that it was a government job. The time schedule was flexible, there wasn't a profit margin, and I was given more to do than if I had worked at IBM. There's something good about government work, even though the standards are lower and there's less super-quality talent. For young people who want a bigger piece of the pie than they can get in industry, all they have to do there is ask for it.

• Did you have a mentor?

Although I never met him personally, Norbert Wiener was my first mentor. I read his books, and what I understood excited me, because he thought about systems and how they worked on a large scale. He covered statistical mechanics, neurophysiology, and control theory, and tied them together to see what they had in common. Back then, I didn't understand the math very well, but his broad, technical inquiries were wonderful.

The first three mentors whom I knew personally served on my thesis committee at Berkeley—Professors Charlie Desoer, Leon Chua, and George Oster. Charlie was excellent at circuits and feedback systems, especially nonlinear ones. He created an atmosphere in which deep thinking in systems was encouraged. He also provided the glue for many faculty and grad students in a culture that reached out to others in biology, circuits, and economics. It was easier to talk to him than many other system theorists because he didn't demand that you translate a question into mathematicalese. This required him to know the engineering descriptions apart from the math, and to be willing to take the burden of translation off the student's shoulders. Charlie was also a great apostle of clarity. When you thought you had something basically right, he would consider that merely foreground—NOW we start. Leon was excellent at making nonlinear circuits and thinking deeply about their weird behavior. He helped to create a vocabulary and an environment for that, and he provided me with enormous encouragement to publish. Just as Charlie and Leon were into the mathematical parts of a problem and understanding the dynamics of nonlinear systems, George was wonderful in biology and modeling. He created the field of network thermodynamics, where he used nonlinear circuit theory to model complicated, interactive thermodynamic systems. Thermodynamics was originally developed to study things that are thermal yet simple, like a steam engine. If you want to model something complicated, like a human cell, you need a discipline like circuit theory. Circuit theory is great in helping you understand complicated things as an interconnection of simple components. There was a need to model complicated, interactive systems in cells, but no one had done it, and George went a long way in that direction.

• You spent seven years completing your doctorate at Berkeley.

If you had mathematical interests in the behavior of circuits and systems, even biological systems, it was a wonderful time to be at Berkeley. It was cheap back then, and probably still is. I think tuition was $350 a quarter. So, one could afford to learn things deeply. Many of us spent years working through real analysis courses as a side interest, but our own work was either engineering or biology. Rather than taking the attitude, "I've got to get out of here, so I'll learn the minimum aside from my discipline," you could say, "I'll devote eighteen months to getting real analysis under control, then take a couple of more courses a quarter for four consecutive quarters." I went there with a master's degree, and took more than twice the course load required for a doctorate for students who arrived there with a bachelor's. I did all the pre-med requirements except second-quarter organic chemistry and genetics. I did everything for a master's in math, except the thesis. At that point, I was tired of graduate school, so I wrote up my dissertation and bought a one-way ticket to Cairo, Egypt. Luckily, I brought along enough traveler's checks to make it back four months later.

• ***Were you still considering a career in medicine?***

I probably should have gone to med school, but after Berkeley, I was tired. I just couldn't think of putting aside the previous five years of research for another eight years while I did an MD, an internship, and a residency. I had worked in Highland Hospital in Oakland as a volunteer. Ultimately, I found it overwhelming to deal with the patients who came in from knifings and gun fights. I couldn't see fixing it, nor could I see an end to it. It was also terrible to be with people in areas where they were so afraid. I wasn't drawn into doing that for forty more years when I couldn't change it. My dad was a doctor in internal medicine, and his dad before him was a physician. My dad was also knowledgeable in cardiology and he was one of Tennessee's leading experts in tropical diseases, having served four years in the army in Panama. He was more involved with people than I am, and very empathetic. I can inspire people intellectually, but I'm not as good at understanding their deep, personal fears. Probably, I would have been a research MD rather than a clinician.

Following Berkeley, I did a postdoc at the Medical College of Virginia with Professor Don Mikulecky, who modeled membrane transport in cells. I had reviewed his papers as a grad student and I liked his work, so I called him up. He invited me for a postdoc and I worked one year in the department of physiology. Eventually, I realized that I wanted a regular job. When I looked around, there were only a few intellectually good organizations that were in interesting places. It came down to Columbia and MIT. I came within minutes of going to Columbia, but MIT called just in time, and I accepted an assistant professor position.

• ***After returning to MIT in 1979, you worked with Professor William Siebert in RLE's Biophysics Group.***

Bill Siebert was my mentor at that time. He helped me find my way around MIT and to understand how things worked here. We had a joint interest in thermodynamics and its analytic basis in terms of circuit theory and random stochastic processes. He and I still share interests in signal processing, thermodynamics, and biological modeling. He worked with me to supervise Han-Ngee Tan's 1984 dissertation. We used circuit theory and random processes to understand how electrical circuits driven by thermal noise behaved like other thermodynamic systems. It's usually understood in a macroscopic way, like steam and power, but we were interested in the microscopic level, and came up with new results and a good paper. We found an extension of the second law of thermodynamics to the frequency domain representation of random noise. It didn't require the noise to be thermal, and that was new. Then, we set up an analytic framework which allowed us to produce a thermodynamic description of noise in nonlinear circuits. The description worked and made sense, not only away from equilibrium (where most of thermodynamics fails), but also away from steady state. It was hard to get answers in closed form, but the equations were exactly right even during violent transients. That was such a relief compared to classical thermodynamics where, once things became nonequilibrium or nonsteady state, the concepts failed. In our treatment, they didn't fail.

• ***How did you become interested in nonlinear theory?***

I was tired of linearity, Fourier transforms, and all the tools used by electrical engineers. It seemed like a spent language with overused verbiage. That's not quite true since there still is new and interesting work to do in linear systems, but much of what electrical engineers do is not interesting. In nonlinear theory, none of the verbiage works, so you need to start fresh. The tools are few, the problems hard, and you aren't using up the language created by others. Nonlinear systems have interesting phenomena—they can serve as storage media, they can oscillate, they can go chaotic, they can blow off into infinity, and they can have multiple and different oscillations depending on where you start. Also, many biology problems are nonlinear. It isn't a question of what you prefer, it's a question of how the system acts. If you linearize it, you miss the problem.

• ***What attracted you to research in machine and human vision?***

Initially, I did a bachelor's project in neurophysiology at MIT with Murray Eden. Then, at Berkeley, I began my doctoral work with Frank Werblin, who was a bioengineering professor in the electrical engineering department. He worked on intracellular microelectrode recording in the retina. Although I wasn't the world's best experimentalist, I was left with an interest in how cells in the eye can process information and with a respect for how hard it is to do these experiments. In postdoc research, I used circuit models to represent transport phenomena in cell membranes, but there was nothing neural or visual about it.

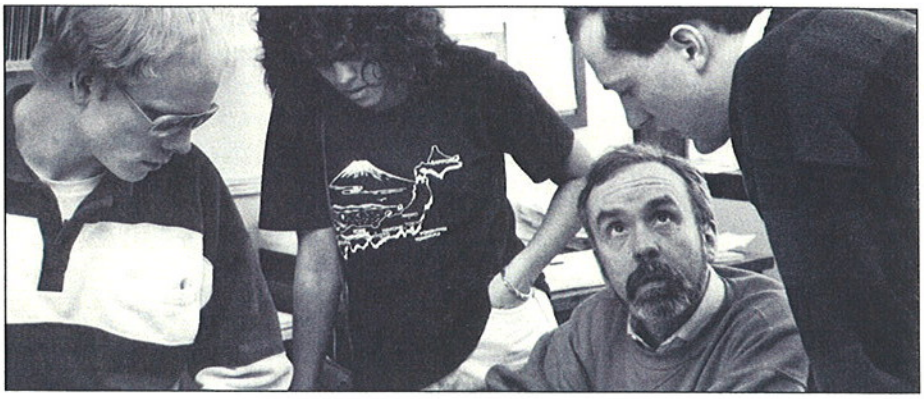
After I returned to MIT in 1979, the field of neural networks or artificial neural systems began to arise. I took a leave of absence for one semester to study neural nets at Lincoln Lab and Caltech. Carver Mead's neural nets work at Caltech interested me. He used circuits loosely modeled on the behavior of the nervous system, to do information processing. They were building chips to do vision, and his artificial retina designs inspired me. He had come to MIT to give a talk, and I had approached him afterwards to tell him that's exactly how we ought to be using silicon. I had it in my mind, from my work with Frank Werblin, that silicon should be used to make retinas and arrays that responded to light and did on-chip processing. All the digital research with silicon seemed to be in a completely different spirit from that. Carver had the knowledge and the revolutionary desire to do something different. After working at Lincoln, I visited Carver's group at Caltech for two months and returned to Lincoln to teach what Carver was doing.

I was inspired by Carver's group, and I felt we needed to do that kind of work at MIT. His shouldn't be the only group working on analog VLSI for vision. So, that's why I started the vision chip project. In analog microchip design, we have better talent than the Caltech group—Harry Lee and Charlie Sodini—and we have our own fabrication facility. Charlie is our fab expert and Harry is our circuit design expert, and they know enough about each other's area. I began to talk to other people

at MIT, like Tommy Poggio and Berthold Horn, and we began work on the MIT Vision Chip Project.

Our approach differs from Carver's. His is based on the nervous system. We simply build analog systems. Carver is inspired to learn analog circuit design that copies the nervous system, and we're inspired to use analog circuits for new engineering applications of vision. Carver also does continuous-time CMOS circuits in subthreshold modes. This involves very tiny currents where the transistors work exponentially. We don't operate there, partly because those systems run slow, and partly because transistor matching is so poor. Also, we do things utterly unlike what Carver does, like charge coupled devices (CCDs). We aim for engineering performance. In the long term, he does too, but we're not interested so much in the nervous system. At MIT, there are no experts in analog circuit design *and* neurophysiology, so we have to build the project around the people we have, how they think, and what they like to do.

The vision chip project has worked out well. We've designed and built very fast chips; 1,000 frames per second is normal in our work. We believe we can design analog chips that work at speeds about two orders of magnitude higher than digital, with power two orders of magnitude lower than digital, and cheaper than digital because the chips are smaller when manufactured in quantity. At the same time, they're special purpose and not programmable like a digital chip. One of our doctoral students has designed a chip that does on-chip filtering and produces an image that looks like an edge map. The chip is an ordinary CCD camera with on-chip processing at 1,000 frames per second. Another student has designed a camera chip that determines the position of a bright object and its orientation within a scene at 5,000 frames per second. That's a single-chip system. Yet another student has designed a CCD system that simplifies images by preserving the edges but smoothing out the gray areas. We have other single-chip systems that are being tested or designed, as well as other chips that test particular technologies, but they're not complete systems on a single chip.



Professor John L. Wyatt, Jr. (seated) compares notes with graduate students (from left): Mark N. Seidel, Malini V. Narayanan, and Paul R. Pilotte. (Photo by John F. Cook)

- ***Does the vision chip project have any application to artificial intelligence?***

Our work doesn't relate to traditional artificial intelligence, which works with *highly processed* data that already make logical sense. We work with *raw* data that describe the world and determine how we can make sense of that data. We model the eyes and the early visual parts of the brain that find edges, determine motion, and find form. The applications we have in mind for the vision chip project are automatic manufacturing and vehicle navigation, where it is important to quickly sense objects visually—fast enough to guide a robot arm that's doing a quick job.

- ***What is involved in your other project, the implantable retina chip?***

The group of people I work with includes Dr. Dave Edell (a principal research scientist from the Harvard-MIT Division of Health, Sciences, and Technology), who consults for Lincoln Lab, and Dr. Joe Rizzo, MD (an ophthalmologist and neurologist from the Massachusetts Eye and Ear Infirmary). For many years, Joe has worked on retinal transplants in animals. The hope is that someday this procedure can be used to restore the function of damaged retinas in humans. It's technically successful, but there's currently no hope for connecting a transplanted retina to the brain. Joe thought there may be some way to assist a damaged retina electronically. He asked if we could design a chip to place in the eye, and I told him probably not. How do you get power into the chip without wires hanging out and risking infection? How can you put anything up against the retina without wrecking it? The retina has the mechanical consistency of a single layer of wet tissue paper, and it doesn't want you to mess with it. Furthermore, it's not firmly attached to the back of the eye. So, it's a difficult place to work.

Fortunately, the retina is built backwards in the eye and it's all very transparent. The receptor cells are on the retina's edge farthest from the lens, and the output or ganglion cells are nearest the lens. There are two illnesses in which the receptor cells die, but the output cells apparently continue to work—retinitis pigmentosa and macular degeneration. Approximately 10 million people in the U.S. suffer from these two forms of blindness and more than 400,000 are legally blind. Since the output cells continue to function in both illnesses, it's theoretically possible to drive them with an implantable microchip with an array of electrodes. Human cells can be driven electrically. We don't have to penetrate the cells with electrodes, all we have to do is put an electrode near them (closer than 50 microns) and pulse the electrode with voltage at the right polarity. The cells will fire as if they were driven through synapses in a healthy retina.

It is amazing how good modern integrated circuit technology is. The diameter of ganglion cell bodies in a human is about 30 microns. With modern commercial fabrication, we can produce individual features, such as the width of a piece of wire, as small as 0.6 micron. So, a cell in the eye is about fifty times bigger than a structure made with commer-

cially available chip technology. It is possible to cover a single human cell with lots of these fabricated structures. Our goal is to make an electrode array, using new techniques to stimulate the ganglion cells, that can gently sit on the retina and provide some degree of vision.

There are many difficulties. First, the retina is extremely pressure-sensitive. Pressure as little as 10 millimeters of mercury can produce blindness, and that's pressure mediated gently through a fluid. You could imagine putting a brick of a microchip up against the retina and somehow attaching it. The retina would not like it any more than you would like being caressed by a bulldozer! We must find ways to gently attach the array so it doesn't sit like a concrete block on the retina. There are also chemical forms of toxicity. If we were to insert very small quantities of copper or iron in the eye, the retina would be completely destroyed. In addition, the electrical driving process produces electrochemical products that can well be toxic. So, we have mechanical toxicity from the pressure, chemical toxicity from the substances placed in the eye, and electrochemical toxicity from the driving process. Plus, there's surgical damage simply from entering the eye and the possibility of rejection. Those issues alone make it a difficult problem.

Right now, I don't know the likelihood of the project's success. But since it can help such a large population, I think we must take the risk. Either it won't work at all, or it will work after a prodigious effort. It may not provide good vision any time soon, but the difference between total blindness and the ability to see one's way around just a bit is very important.

- ***What is the biggest obstacle to your research?***

My biggest obstacle is that I'm primarily involved in practical projects when my own research is theoretical. So, I've created a situation for myself where I'm a fish out of water. The vision chip project is largely about design, building, and testing chips, although there are some theoretical notions about using linear-nonlinear resistive grids as parallel image processing machines. Similarly, the retina chip project has no theory in it right now. It's all biological experimentation. The up side is that I saw these things which needed doing, and I put together the groups to do them. These two projects are important because they bring people together in interesting, worthwhile lines of work; people who wouldn't necessarily know each other. The down side is that I spend a large amount of time administering and supervising other peoples' research.

In general, the biggest obstacle to any research is time. It seems there's a trend at U.S. colleges and universities to turn researchers into research supervisors. The trend is to take people who are good at research, tenure them on the basis of their contributions (to a significant extent in research), and then cease to reward them for doing the research. Instead, they are rewarded for doing administrative work, bringing in funds, or starting new directions. There are the basics—teaching, acquiring funds, finding graduate students, and sitting on exam committees. By the time all that's done, plus administering and reporting on a project, you've already done a moderately demanding year of work. So, doing your own research is a luxury. I think that's the biggest problem for a university professor. Some people quit and don't do research, others administer research but don't do it themselves. One can get absorbed by the administrative activities within an academic department, especially a large one, because the amount of administrative work grows more rapidly than the size of the department.

- ***How do you see your role as a teacher?***

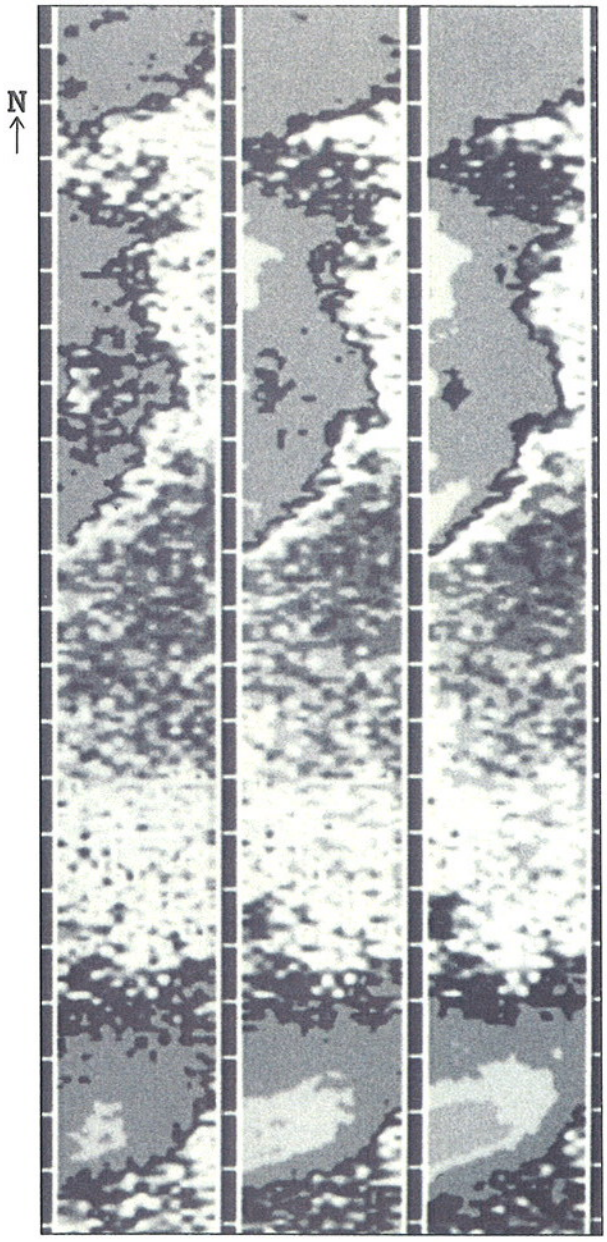
I view the job of a teacher as one of clarifying, at least for graduate courses. That means telling the story in a rough way to get the intuition across, then telling the story again in a precise way to get the math right, and finally tying them together. I try to teach things I don't know very well, though I avoid things that I'm utterly unqualified to teach. Right now, I'm teaching a course on estimation and random processes. I haven't thought about that material in almost two decades. So, preparing to teach it is a real learning experience for me. If you've got to teach, why not make it a learning experience!

- ***What is the future for VLSI?***

The most important thing that has happened in VLSI is the incredible, highly developed fabrication technology, where billions of dollars have been spent to optimize it. The technology is potentially good in many applications, particularly where electricity plays either a small role or no role at all—the microfabrication of accelerometers, small actuators, electric motors and pumps; and in on-chip chemistry applications, such as electrophoresis, which is used to separate out chemical compounds. The application of chips to other things that handle analog data is one of the most interesting things going on—on-chip chemical actuators; sensors for temperature, mechanical pressure, and acceleration; and motors that can move gases around. There are chips with arrays of tiny, electrically controlled mirrors that can reflect light and produce a display. In principle, they can modulate images from space and overcome the effects of atmospheric motion.

As I mentioned before, in the implantable retina chip project, it's amazing that the ganglion cells are about 30 microns in diameter, and the objects that can be fabricated in the modern commercial process are on the order of 0.6 micron in diameter. These feature sizes are already below the biological scale of most human cells. Using this technology to interface to the nervous system is extremely interesting. The digital handling of information on-chip is a well-developed activity, but using analog technology to interface with physical and biological media, and to do chemistry on chip is a new and exciting process. A company in California uses this technology to grow proteins in a 100x100 array of cells—10,000 different ones on a single chip—with no electricity involved at all. They start to grow the cells and cover a fraction of them. Then, they grow a certain amino acid on the uncovered cells. By programming which cells are covered, they can grow 10,000 different proteins at once and know exactly what each one is. If they want to assay something for a response to a certain antigen, they can do all 10,000 tests at once. This may be of more revolutionary importance in terms of technology than what's been done electrically on a chip.

What About Bob?



High-resolution passive microwave images of Block Island, Rhode Island, as it lies below the storm clouds of Hurricane Bob. The solid-colored semicircle on the upper left of each recording shows clouds normally associated with a hurricane. From left to right, the three magnetic tape strips show data at descending levels of altitude. Changes in temperature are indicated by different colors, and the eye of the storm appears to be warmer than its surrounding area by several degrees. The activity shown on the lower left is a band of rain associated with the storm.

The gray skies and heavy subtropical air over NASA's airfield on Wallops Island, Virginia, testified to the approach of Hurricane Bob on the morning of August 19, 1991. One week earlier, scientists from laboratories across the country had assembled to gather data on convection and precipitation, and the electrification of thunderstorms.

Participants from RLE's Radio Astronomy Group were Principal Research Scientist Dr. Philip W. Rosenkranz, Sponsored Research Staff John W. "Jack" Barrett, and graduate student Michael J. Schwartz. The trio conducts experiments in microwave atmospheric sensing with Dr. David H. Staelin, Assistant Director of Lincoln Laboratory and Professor of Electrical Engineering and Computer Science. Using high-altitude research aircraft and meteorological satellites, they collect data on atmospheric water vapor, ozone, temperature, and surface conditions on Earth.

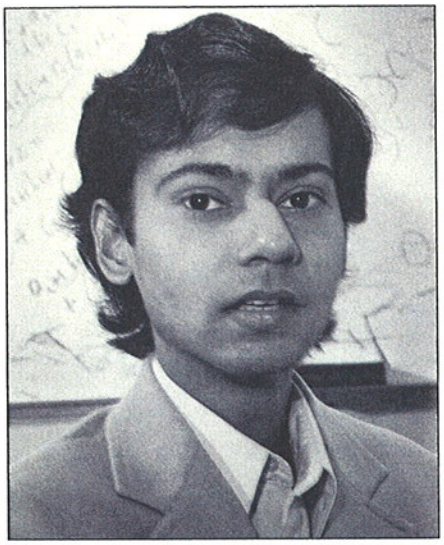
On the morning of the storm, Jack Barrett and Mike Schwartz were hoping to gather additional data with RLE equipment aboard the high-altitude ER-2 aircraft. The plane has flown earlier research missions over thunderstorms south of Cape Hatteras, North Carolina. Since the plane's wingspan was so large, it was now grounded in the face of the impending hurricane. This was not the kind of aircraft suited for windy take-offs and landings.

Later that morning, conditions changed, and clearing skies indicated that Bob's path would miss Wallops Island. The ER-2 quickly took to the skies and caught up with Bob just before it slammed into New England. Hurricanes are normally viewed from space satellite images, and the RLE team did not suspect that Bob would make such an excellent subject for their high-resolution microwave sensing experiment. Their passive microwave methods proved advantageous because they could receive signals from within and below cloud cover; other techniques would not have penetrated the cloud tops. The microwave instrumentation on board the ER-2 was built at RLE and consisted of a series of receivers sensitive to the 5- and 3-millimeter oxygen bands in the atmosphere. RLE's successful, high-flying mission produced the first high-resolution passive microwave images of a hurricane's center from several kilometers distance, and recorded temperatures at eight different altitude levels.

The RLE Radio Astronomy Group is currently analyzing the data collected from Wallops Island. Aside from the terrible coastal damage left by the storm, their microwave images are all that remain of Hurricane Bob, and represent a bench mark for others to challenge.

by John F. Cook

circuit breakers

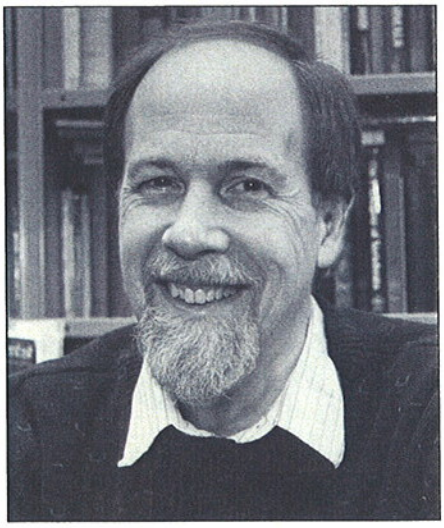


Dr. Srinivas Devadas will be promoted to Associate Professor of Electrical Engineering and Computer Science, effective July 1, 1992. Professor Devadas, a graduate of the Indian Institute of Technology (B. Tech. '85) and the University of California, Berkeley (MS '86, PhD '88), joined the MIT faculty as an assistant professor in 1988. He held the Analog Devices Career Development Professorship from 1989 to 1991. As a faculty member in RLE's Circuits and Systems Group, Professor Devadas explores the synthesis and testing of VLSI circuits and systems, particularly in the areas of test generation and logic synthesis. He has made significant contributions to data path synthesis and logic synthesis and verification. *Photo by John F. Cook.*

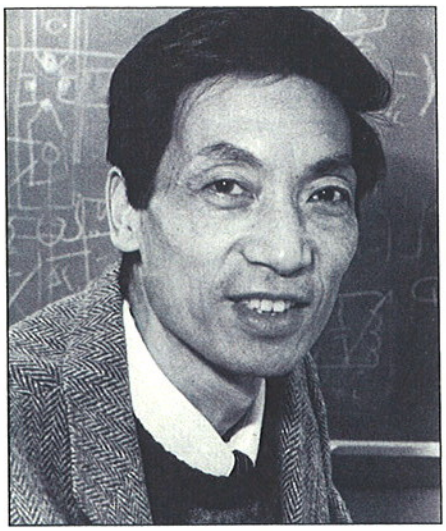
Dr. Leslie A. Kolodziejski, Karl Van Tassel Career Development Assistant Professor, will be promoted to Associate Professor of Electrical Engineering and Computer Science, effective July 1, 1992. Professor Kolodziejski came to MIT as an assistant professor in 1988 from the faculty of Purdue University (BS '83, MS '84, PhD '86). As a member of RLE's Materials and Fabrication Group, she conducts research in materials growth for electronic and optical applications. Her research focuses on the growth of II-VI and III-V materials using chemical beam epitaxy techniques. She also holds a

Dr. Leslie A. Kolodziejski

Presidential Young Investigator Award (1987-92) from the National Science Foundation. *Photo by John F. Cook.*



Dr. John J. Guinan, Jr. (SB 63, SM 64, PhD 68), Principal Research Scientist in RLE's Auditory Physiology Group, was appointed Associate Director of the Eaton-Peabody Laboratory at the Massachusetts Eye and Ear Infirmary, effective January 28, 1992. Dr. Guinan has been affiliated with RLE since 1963, and conducts experimental research on the mammalian efferent system, which the central nervous system uses to control incoming messages from the ear to the brain. His research has furthered understanding of the processes involved in hearing, particularly how the central nervous system responds to sound, and has demonstrated that the concepts associated with man-made engineering systems can be applied to the study of the nervous system. Dr. Guinan is a member of the American Association for the Advancement of Science, the Federation of American Scientists, the Acoustical Society of America, and the Society for Neuroscience. *Photo by John F. Cook.*



Mr. Qizheng Gu was appointed Research Scientist in RLE's Center for Electromagnetic Theory and Applications, effective February 1, 1992. As a visiting scientist in RLE since 1983, Mr. Gu has conducted research in electromagnetic interference modeling of receivers for precision aircraft landing systems and the theoretical analysis of transient signal propagation and interference in high-speed integrated circuits. From 1962 to 1983, he was senior engineer and deputy director of the Research Department at Shanghai Xinhua Radio Factory. He has also served as professor and deputy director of the Research Laboratory of Electrical Engineering at Shanghai's Research Institute of Mechanical and Electrical Engineering since 1987. Mr. Gu graduated from Fudan University in Shanghai in 1960. Since 1978, he has received four Awards of Important Science and Technology Achievements from the People's Republic of China. *Photo by John F. Cook.*

alumni notes

Corine A. Bickley (PhD '87), Visiting Scientist in RLE's Speech Communication Group and Lecturer at MIT's Writing Program, teamed up with undergraduate Thomas R. Westcott ('93) of RLE's Sensory Communication Group to teach an American Sign Language seminar at MIT. The seminar not only included sign language instruction, but also addressed the sociological issues of deafness and technological advances in aids for the deaf.

William T. Dyall (SM '48) is keeping the staff of ***currents*** on its toes. As a member of the Society for the Preservation of English Language and Literature (SPELL), he has become ***currents'*** unofficial "goofreader." Mr. Dyall is retired from Sierra International and lives in Los Altos, California.

Raymond M. Redheffer (SB '43, SM '47, PhD '48), retired Professor of Mathematics at UCLA, writes from his home in Los Angeles. In November 1991, Dr. Redheffer received an honorary doctorate in mathematics from Karlsruhe University in Germany, the first conferred in 31 years. Dr. Redheffer was a member of the MIT Radiation Laboratory (1942-46) and RLE's antenna group (1946-48).

According to *The Boston Globe* of February 7, 1992, ***Robert J. Shillman*** (SM '72, PhD '74), "colorful entrepreneur and president of Cognex Corporation of Needham, rented out the JFK Library last night to hand out $500,000 in bonuses to 130 employees. A George Bush impersonator was on the program for added levity."

Thomas E. Stern (SB/SM '53, ScD '56), Dicker Professor and Chairman of Columbia University's Department of Electrical Engineering, recalls many familiar names and faces that appeared in the fall 1991 issue of ***currents***. Since 1985, he has served as Technical Director of Columbia University's Center for Telecommunications Research, and conducts research in optical communication networks. Columbia's Electrical Engineering Department will celebrate its centennial this year, and Dr. Stern writes, "That's one of the things that put me in the mood to reminisce."

Both ***Stewart D. Personick*** (SM '68, EE '69, ScD '70) and ***Charles L. Seitz*** (SB '65, SM '67, PhD '71) were elected to the National Academy of Engineering. Dr. Personick is Assistant Vice President of Bell Communications Research, Inc. in Morristown, New Jersey, and Dr. Seitz is on the computer science faculty at the California Institute of Technology in Pasadena, California. They joined thirteen other MIT alumni and two MIT faculty members who were recently elected to the academy, one of the highest professional honors for an engineer.

RLE congratulates the following alumni for awards recently presented by the Institute of Electrical and Electronic Engineers:

C. Gordon Bell (ScD '53), a computer industry consultant, received the 1992 John von Neumann Medal.

John H. Cafarella (SM/EE '73, ScD '75), partner in Micrilor, Inc. of Wakefield, Massachusetts, was elected to Fellow in the IEEE Signal Processing Society.

G. David Forney, Jr. (SM '63, ScD '65), Vice President at Motorola Codex Corporation in Mansfield, Massachusetts, was awarded the 1992 Edison Medal. The medal is presented for a career of meritorious achievement in electrical science or engineering.

Thomas S. Huang (SM '60, ScD '63), Professor of Electrical Engineering at the University of Illinois/Champaign-Urbana, was honored by the IEEE Signal Processing Society with its 1991 Society Award for contributions and leadership in the areas of image and multidimensional signal processing.

James L. Massey (SM '60, PhD '62), Professor of Digital Systems Engineering at the Swiss Federal Technical University in Zurich, Switzerland, received the 1992 Alexander Graham Bell Medal. The medal is awarded for exceptional contributions to the advancement of telecommunications.

Ronald W. Schafer (PhD '68), Institute Professor at the Georgia Institute of Technology, was named recipient of the 1992 Education Medal. He was cited for excellence in curriculum development, teaching, and textbooks in digital signal processing and digital speech processing. Dr. Schafer joins other distinguished RLE alumni as previous Education Medal winners: Institute Professor Hermann A. Haus (ScD '54) in 1991, Professor Alan V. Oppenheim (SB/SM '61, ScD '64) in 1988, and Professor Emeritus Robert M. Fano (SB '41, ScD '47) in 1977.

Publications

RLE has recently published the following technical reports:

Adaptive Matched Field Processing in an Uncertain Propagation Environment, by James C. Preisig. RLE TR No. 567. January 1992. 173 pp. $17.00.

Theory of Resistive and Ideal Internal Kinks, by Stefano Migliuolo. RLE TR No. 568. February 1992. 83 pp. $15.00.

Modeling Speech Perception in Noise: The Stop Consonants as a Case Study, by Abeer A.H. Alwan. RLE TR No. 569. February 1992. 133 pp. $16.00.

Spread Spectrum Modulation and Signal Masking Using Synchronized Chaotic Systems, by Kevin M. Cuomo, Alan V. Oppenheim, and Steven H. Isabelle. RLE TR No. 570. February 1992. 39 pp. $10.00.

Probabilistic State Estimation with Discrete-Time Chaotic Systems, by Michael D. Richard. RLE TR No. 571. March 1992. 90 pp. $12.00.

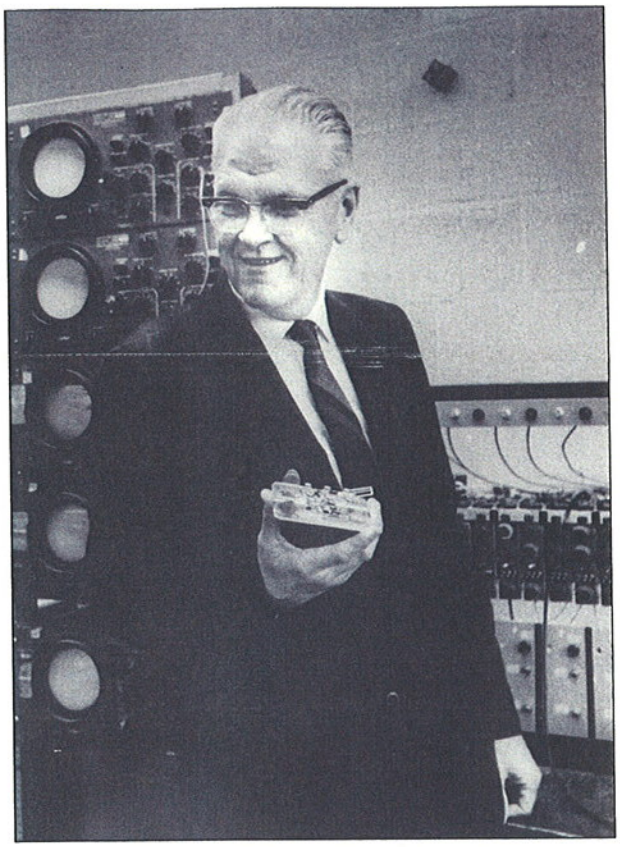
A New Approach to Parameter Optimization of Products and Manufacturing Processes, by Ashraf S. Alkhairy, RLE TR No. 572. Price to be announced. Available in September 1992.

In addition, ***RLE Progress Report No. 134,*** which covers the period January through December 1991, provides extensive information about the research objectives and projects of RLE's research groups. It also lists faculty, staff, and students who participated in each research project, in addition to current RLE personnel, and identifies funding sources. The ***Progress Report*** is available for $5.00 (to U.S. addresses) and $9.00 (to foreign addresses) to cover postage and handling.

Ordering information is on back cover.

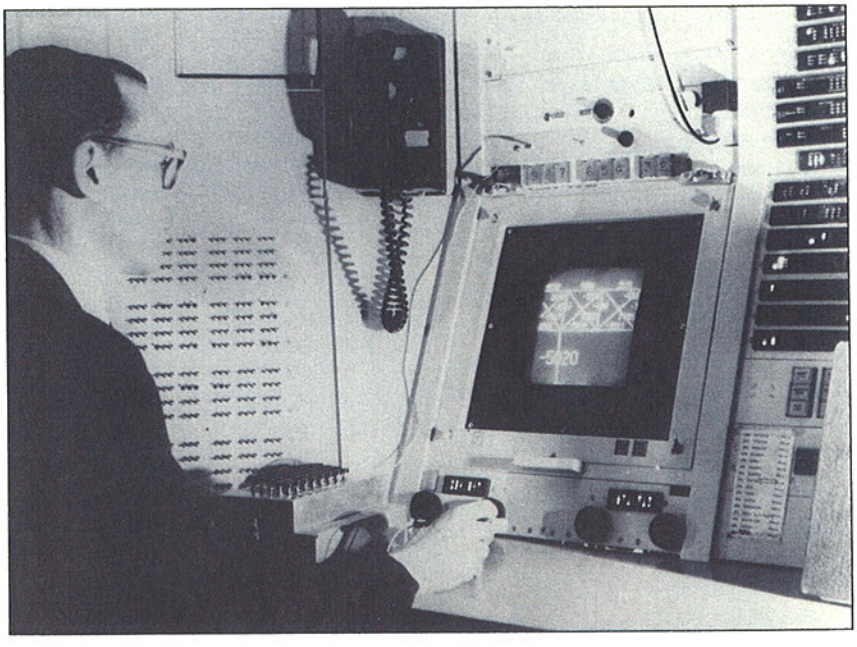
History of VLSI Computer-Aided Design at RLE

"Although there was a great deal of activity in RLE in the early 1960s in characterizing semiconductor devices and circuits, MIT did not participate strongly in the early development of integrated circuits as opposed to the study of discrete devices. In 1978, however, Professors Jonathan Allen and Paul Penfield recognized that important new design techniques, focused on MOS (Metal-Oxide-Semiconductor) circuits, had opened up the possibility of designing large circuits at a system level with impressive performance. Building on a semester visit by Ms. Lynn Conway of the Xerox Palo Alto Research Center, a robust new activity in integrated-circuit design built up, spanning interests all the way from the device level to large complex computing systems. The emphasis in RLE has been on the building of a number of software design tools, many of which are used extensively in industry, and on the development of new circuit-analysis techniques and high-performance architectures for digital signal processing."—A Century of Electrical Engineering and Computer Science at MIT, 1882-1982 *by Karl L. Wildes and Nilo A. Lindgren*



1954

Professors Henry J. Zimmermann, Samuel J. Mason, and Richard B. Adler were part of a group in RLE that investigated the fundamental principles of transistor circuit design and their practical application in communication engineering. The study of noise in semiconductors was also related to this research. Professor Zimmermann is shown here in a 1975 photo. (Photo by Ivan Massar/Black Star)



1962

MIT doctoral student Ivan E. Sutherland (PhD '63) developed Sketchpad, an interactive computer graphics program that was implemented on Lincoln Laboratory's TX-2 computer. By the mid-'60s, major American corporations were conducting research on interactive computer graphics. (Photo courtesy of Lincoln Laboratory)

1950s/1960s

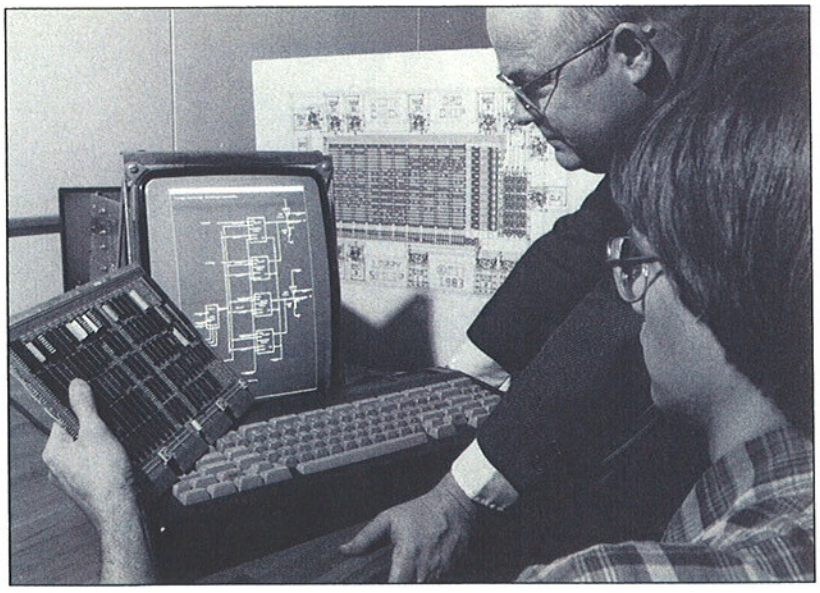
Professor Richard D. Adler was a member of RLE since its inception in 1946. From 1951 to 1953, he was the leader of Lincoln Laboratory's first solid-state and transistor group. Along with Professors Samuel J. Mason, Carl R. Hurtig, and Walter E. Morrow, Jr., he pioneered the development of a new nonlinear circuit model for point-contact transistors. From 1960 to 1968, he served as technical director of the Semiconductor Electronics Education Committee (SEEC), an international university- and industry-sponsored educational development effort. The SEEC successfully introduced solid-state electronics into university curricula by producing seven textbooks, pedagogical lab experiments, and four educational films on the subject. Other members of the SEEC included Professors Campbell L. Searle, Paul E. Gray, Arthur C. Smith, and Richard D. Thornton. Professor Adler is shown lecturing in a 1963 photo (courtesy MIT Museum) and Professor Thornton examines a component in a 1975 photo (Ivan Massar/Black Star).

Winter 1978

In January 1978, about 25 MIT faculty members and scientists participated in an intensive LSI design workshop. The challenge was for the workshop participants to become the foundation of MIT's new thrust into integrated circuit design. Just as the avalanche of new information concluded, the workshop was commemorated by New England's blizzard of 1978, which closed MIT for a week and gave the attendees some time to reflect and complete their take-home final exam. (Photo by Stephen L. Finberg '77)

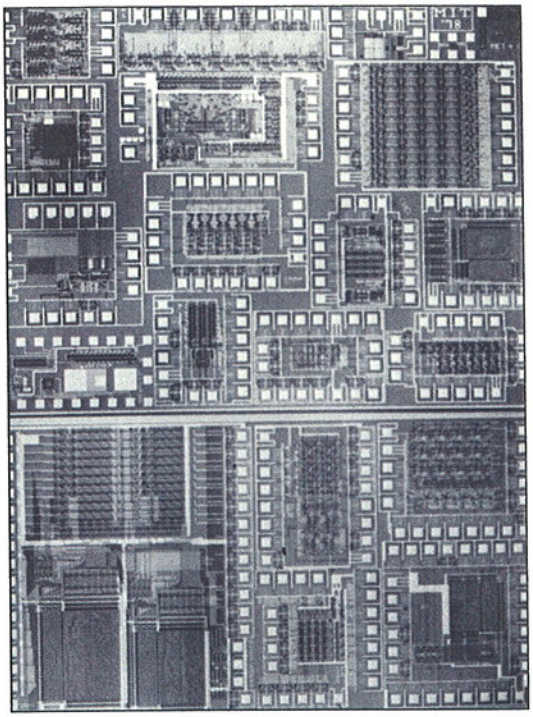
Fall 1978

Visiting Associate Professor Lynn A. Conway introduced MIT students to their first VLSI design course in the fall of 1978. As a researcher from Xerox Palo Alto Research Center, she had collaborated with Professor Carver Mead from the California Institute of Technology on a landmark system-oriented approach to VLSI design. Thirty students enrolled in the new course, which was based on this approach. Professor Conway is now the Assistant Dean of Engineering at the University of Michigan at Ann Arbor. (Photo courtesy of Lynn A. Conway)



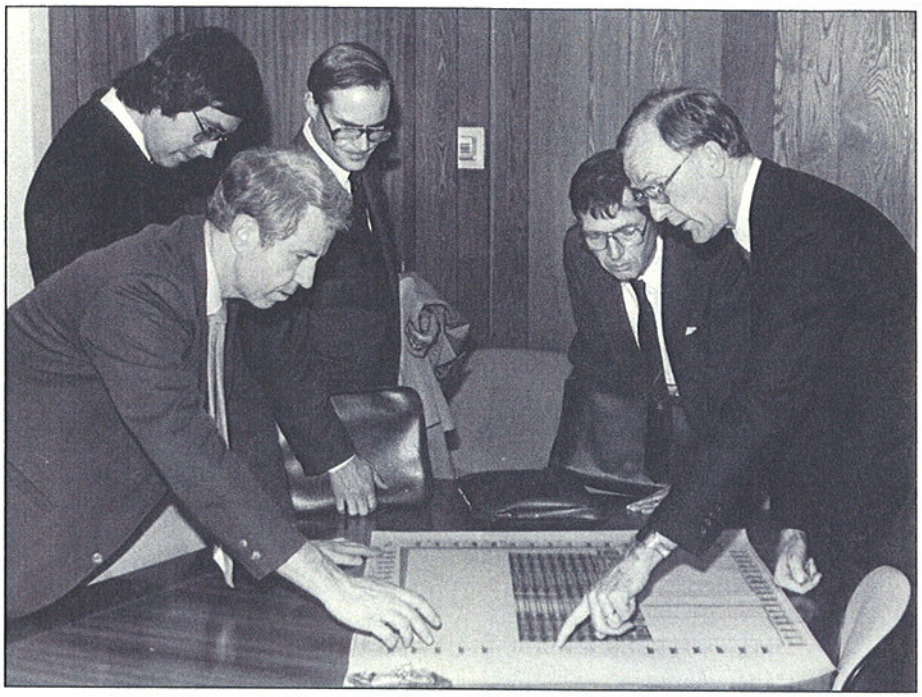
1983

Professor Jonathan Allen and graduate student Larry D. Seiler inspect the design of a system for high-speed design rule checking that uses four custom integrated circuits in a novel architecture. The design rule checker was used in Professor Allen's VLSI design course, which continued the curriculum brought to MIT by Professor Lynn Conway. (Photo by John F. Cook)



Fall 1978

The 1978 MIT Multiproject Chip was the most ambitious multiproject chip to date. Designs were produced by students from Professor Lynn Conway's VLSI design course. This endeavor guided the more extensive multi-university multiproject chip set (MPC79), which involved 124 designers from eight universities. (Photo courtesy of Paul L. Penfield, Jr.)

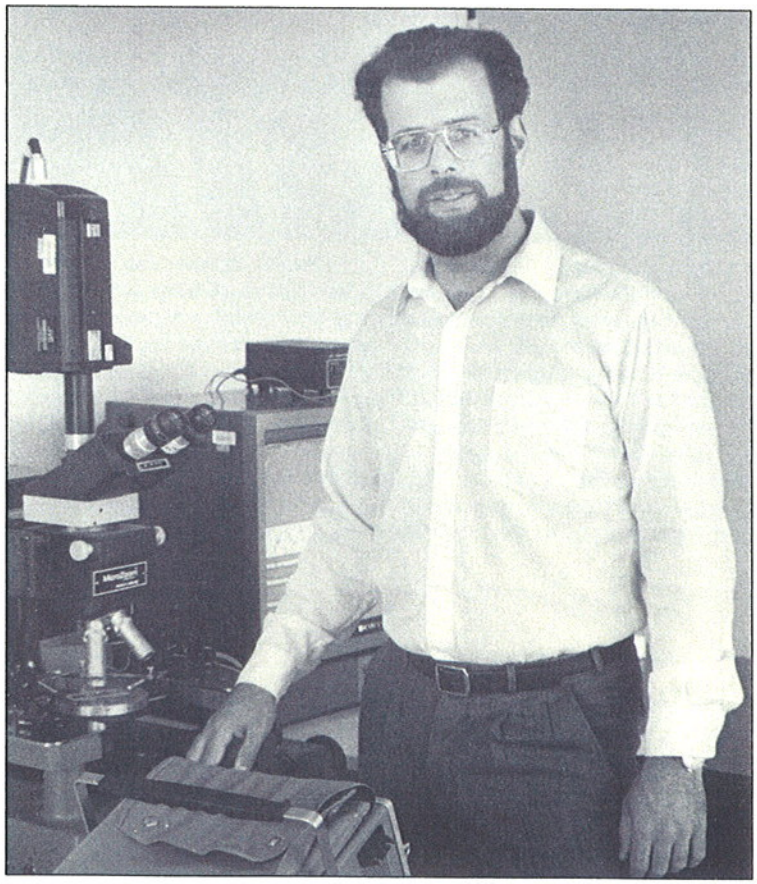


1984

The features of a CMOS chip developed at AT&T Bell Laboratories are examined by (from left) Dr. Michael K. Maul of Bell Labs, Dr. J. Peter Bartl of MIT's Industrial Liaison Program, Dr. W. Dexter Johnston and Mr. Victor A. Vyssotsky of Bell Labs, and Professor Paul L. Penfield, Jr., Director of MIT's Microsystems Technology Laboratories. The same fabrication process used to manufacture this chip would later be used to produce a chip designed by Professor Lance A. Glasser of RLE. (Photo courtesy of MIT Museum)

1985

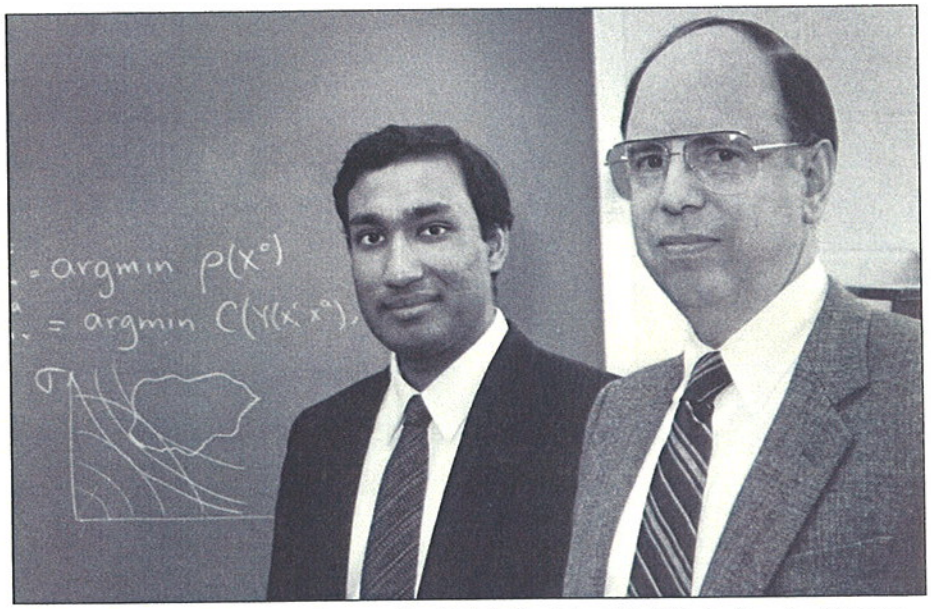
As a principal investigator in RLE's Circuit and Systems Group, Professor Lance A. Glasser studied integrated circuit design and its application in digital VLSI systems, such as massively parallel multiprocessors. His important contributions include research in waveform bounding, a novel ultraviolet write-enable programmable read-only memory (PROM) circuit, and a book which he co-authored, The Design and Analysis of VLSI Circuits. *Currently, he is with the Defense Advanced Research Projects Agency in Arlington, Virginia. (Photo by John F. Cook)*



UPDATE

Industrial Connections

RLE actively promotes innovative relationships between the laboratory and business organizations through RLE Collegium membership, research projects, and special partnerships. The goal is to increase communication between RLE researchers and industrial professionals in electronics and related fields.



Working with Professor David H. Staelin (right), Dr. Ashraf S. Alkhairy has developed a novel approach to manufacturing. Dr. Alkhairy's method is a mathematically rigorous approach used to compute system parameters that can optimize quality in product and manufacturing process development. The number of experiments needed to implement the approach can be an order of magnitude smaller than those required by other methods. Since June 1991, it has been in use at Hewlett-Packard's Avondale, Pennsylvania facility, which produces chromatographic columns, and at their San Diego, California operation since November 1991. This system is expected to save up to $3 million for the two Hewlett-Packard sites over a three-year period. Dr. Alkhairy is currently a postdoctoral associate in RLE, and his research in this area is documented in his doctoral thesis, which will soon be available as RLE Technical Report No. 572. (Photo by John F. Cook)

RLE Collegium

The RLE Collegium was founded in 1987, and the annual membership fee is $20,000. Members of MIT's Industrial Liaison Program can elect to apply a portion of their ILP membership fee to the RLE Collegium. Collegium members have the opportunity to develop close affiliations with the laboratory's research staff, and can quickly access emerging results and scientific directions. Collegium benefits include access to a wide range of publications, seminars, and laboratory visits. For more information on the RLE Collegium, please contact RLE Headquarters or the Industrial Liaison Program at MIT.

Daimler-Benz and McDonnell Douglas Join RLE Collegium

Daimler-Benz of Stuttgart, Germany, renowned for its Mercedes-Benz vehicle division, has joined the RLE Collegium. In 1886, Gottlieb Daimler and Karl Benz produced their first motor cars, and the two companies merged in 1926. Today, Daimler-Benz is positioning itself to become an international force in high-technology development. It has recently acquired the AEG electronics company and formed two new divisions—Deutsche Aerospace and Daimler-Benz Inter-Services. Much like RLE, Daimler-Benz is active in a broad spectrum of research including information technology, new materials and production processes, and artificial intelligence.

The McDonnell Douglas Corporation of St. Louis, Missouri, a world leader in avionics and aerospace technology, recently joined the RLE Collegium. The corporation was formed in 1967 through a merger of the McDonnell Company (founded by the late James S. McDonnell, Jr. '25) and the Douglas Aircraft Company (founded by the late Donald W. Douglas '17). McDonnell Douglas is the world's second largest deliverer of commercial aircraft and the largest U.S. military contractor, with the broadest base of products of any other aerospace company in the world. McDonnell Douglas offers a wide range of products and services that includes everything from training and launch systems to the Space Station Freedom.

RLE welcomes inquiries regarding the laboratory's research. To request an RLE ***Progress Report,*** an RLE ***Collegium Prospectus,*** or for more information on other RLE publications, please contact:

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