Chapter 3. Computer-Assisted Prototyping of Advanced Microsystems

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3.1 Advanced Modeling and Computational Prototyping

Sponsor

Defense Advanced Research Projects Agency
Contract DABT 63-95-C-0088

3.1.1 Modeling of Interconnect Reliability

Project Staff

Yonald Chery, Professor Carl V. Thompson, Professor Donald E. Troxel

Recent research has demonstrated interconnect failure due to electromigration effect to be strongly dependent not only on current density but also on metal film crystal grain size distribution and geometries of interconnect patterns. This type of failure is manifest as a depletion of interconnect metal forming a “void” (open-circuit) or an accumulation possibly forming a “short” to neighboring interconnect.

Our research work focuses on:

1. Developing abstract, physically-based, microstructural interconnect failure models to more accurately predict electromigration induced failure, and
2. Electromigration reliability for network interconnect (ERNI), our prototype computer-aided design tool based on these abstracted microstructurally based models.

A release of ERNI 2.0 is expected soon with extensions supporting hierarchical designs and utilizing higher performance circuit simulation engines. This release will incorporate client and server programs implemented in Java. With this software, multiple designers at different locations will be able to cooperatively design integrated circuitry which incorporates electromigration reliability models.

3.1.2 Modeling of Advanced Device Structures

Project Staff

Zachary K. Lee, Michael B. McIlrath, Professor Dimitri A. Antoniadis

As MOSFETs are scaled to the sub-100 nm regime and beyond, the two-dimensional (2-D) distribution of dopants becomes a very important factor affecting their performance. For example, the reverse short channel effect (RSCE), believed to be caused by the enhanced diffusion of dopants near the source/drain junction regions,[1] is a 2-D problem that directly affects device characteristics. Moreover, the recent development of devices having lateral doping features in the channel and source/drain regions such as halos or pockets[2] also requires an understanding of how dopants diffuse in 2-D during the fabrication process. A technique that allows one to obtain the 2-D doping profile is therefore essential. Immediate

1 S. Crowder, P. Rousseau, J. Snyder, J. Scott, P. Griffin, and J. Plummer, “The Effect of Source/Drain Processing on the Reverse Short Channel Effect of Deep Sub-Micron Bulk and SOI nMOSFETs,” *IEEE IEDM Tech. Dig*. 95: 427 (1995).

2 B. Yu, C.H.J. Wann, E.D. Nowak, K. Noda, and C. Hu, “Short-Channel Effect Improved by Lateral Channel-Engineering in Deep-Submicrometer MOSFETs,” *IEEE Tran. Electron. Devices* 44(4): 627-34 (1997).

applications include process calibration, process monitoring, and process troubleshooting, as well as device design and optimization.

A number of techniques that determine one-dimensional (1-D) doping profiles have been developed and are widely used. Among these are the various C-V methods and secondary ion mass spectroscopy (SIMS). Direct techniques for determining 2-D profiles, such as scanning capacitance microscopy,[3] however, are less mature at the moment. Inverse modeling[4] provides an alternative and practical solution for this problem. In inverse modeling, the objective is to find a doping profile such that its electrical behavior, obtained through numerical simulations, matches its experimentally determined counterpart.

The use of C-V data to extract 2-D doping profiles has been reported. However, due to the extremely small dimensions and capacitance of modern submicron devices, special test structures are needed. Noise and parasitic capacitance also become important issues. In light of these difficulties, we have developed a new technique based on subthreshold I-V characteristics to extract 2-D doping profiles, which naturally includes the metallurgical channel length. By using reliably extracted profiles, which eliminate device structural ambiguities, it is possible to evaluate and calibrate transport models needed for accurate device modeling in the high current regime.

The technique is based on obtaining a 2-D doping profile such that the simulated subthreshold I-V characteristics, over a broad range of bias conditions, match the corresponding experimental data. The basic tool required is a 2-D device simulator embedded in a nonlinear least-square optimization loop which minimizes the RMS error between the simulated and experimental data.

The 2-D profiles are represented using a sum of 2-D Gaussian functions (representing the source/drain/halo), and a 1-D B-spline or Gaussian function (representing the depth-wise variation of the channel not included in the 2-D Gaussian functions). Other basis functions such as the complementary error function and exponential function may also be used, although it was found that the Gaussian functions often produced the best results (i.e., lowest RMS errors). During optimization, the parameters representing the 2-D profile are varied until a best-fit is achieved. Since the subthreshold I-V characteristics are primarily a manifestation of the device electrostatics, which are determined by dopings in the channel and near source/drain extensions, the deep source/drain junctions commonly used to form the source/drain contact areas are not included in the simulations. The only structural information needed *a priori* includes the gate width, gate dielectric thickness, and dielectric constant. However, the gate width need not be specified very accurately for accurate results. Moreover, the channel length, which is determined by the 2-D doping profile, is automatically obtained in the optimization. The gate electrode length, which has little effect on the subthreshold I-V characteristics, need not be known. The gate material is assumed to be metallic. Any polysilicon depletion or quantum mechanical effects are absorbed into an equivalent oxide thickness, obtained by extrapolating regular C-V data to the weak-inversion region.

Thesis

Lee, Z.K. *A New Inverse-modeling-based Technique for Sub-100-nm MOSFET Characterization.* Ph.D. diss. Department of Electrical Engineering and Computer Science, MIT, November 1998.

3.2 Distributed Collaborative Design and Prototyping Infrastructure

Sponsors

Defense Advanced Research Projects Agency
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Stanford University

3.2.1 Distributed Design and Fabrication Architecture

Project Staff

Professor Duane S. Boning, Michael B. McIlrath, Professor Donald E. Troxel

3 R.N. Kleiman, M.L. O'Malley, F.H. Baumann, J.P. Garno, and G.L. Timp, "Junction Delineation of 0.15 mm MOS Devices Using Scanning Capacitance Microscopy," *IEEE IEDM Tech. Dig.* 97: 691 (1997).

4 Z.K. Lee, M.B. McIlrath, and D.A. Antoniadis, "Inverse Modeling of MOSFETs using I-V Characteristics in the Subthreshold Region," *IEEE IEDM Tech. Dig*. 97: 683 (1997); N. Khalil, J. Faricelli, D. Bell, and S. Selberherr, "The Extraction of Two-Dimensional MOS Transistor Doping via Inverse Modeling," *IEEE Electron Device Lett*. 16(1): 17-19 (1995).

The design and fabrication of state-of-the-art semiconductor devices and integrated circuits requires an increasingly diverse and expensive set of resources, including manufacturing equipment, personnel, and computational tools. Advanced semiconductor research activities can be even more demanding, frequently requiring unique equipment and processing capabilities.

We are developing a flexible, distributed system architecture capable of supporting collaborative design, fabrication, and analysis of semiconductor devices and integrated circuits.[5] Such capabilities are of particular importance in the development of new technologies, where both equipment and expertise are limited. Distributed fabrication enables direct, remote, physical experimentation in the development of leading edge technology, where the necessary manufacturing resources are new, expensive, and scarce. Computational resources, software, processing equipment, and personnel may all be widely distributed; their effective integration is essential in order to achieve the realization of new technologies for specific product requirements. Our architecture defines software interfaces and infrastructure based on existing and emerging networking, CIM, and CAD standards. Process engineers and product designers access processing and simulation results through a common interface and collaborate across the distributed manufacturing environment.

Current efforts in this area focus on the application of this architecture to collaborative microfabrication research, distributed process control and process diagnosis, and remote inspection and analysis of microelectromechanical system (MEMS) devices.

3.2.2 Labnet Software

Project Staff

Thomas J. Lohman, Professor Duane S. Boning

University microfabrication laboratories are facing many new challenges and opportunities: facilities are becoming more expensive and difficult to manage; resources and expertise need to be shared and made available to a wider community; education and research are becoming more dependent on multi-institutional collaboration. Given the above challenges, there is a growing need for a new distributed information infrastructure that will allow remote collaboration, access to remote sites' data and sharing of end-user software applications in the face of differences between remote sites in computer platforms, operating systems, and technical resources. Past research has been done within this application domain but most working systems are too tightly coupled to their local facilities, suffer from portability problems, and have never addressed the issue of data distribution and remote site interaction.

The Labnet Software Project was initiated in recognition of a need for universities to share the development and support effort needed to develop and maintain new distributed laboratory information systems. Joint development work among MIT, Stanford University, and the University of California at Berkeley is in progress.

Currently, the three universities are in the initial stage of deploying core software modules at each site in order to initiate testing and user feedback with the intended goal of phasing out existing systems by the end of the decade. The main goals of the project are to:

- Assess and adopt the use of emerging technologies such as the Object Management Group's (OMG) common object request broker architecture (CORBA), OMG's interface definition language (IDL), Sun Microsystems' Java language, and both object and relational databases.
- Create an infrastructure that will enable collaborative distributed design and fabrication (including object-oriented distributed programming interfaces and web-based user interface capabilities).
- Develop abstract specifications of programming interfaces to both data and services, easing the burden of future additions and changes to the software

3.2.3 Process Control System Architecture

Sponsor

National Institute of Standards and Technology/
Advanced Technology Program with On-Line Technologies

Project Staff

Aaron E. Gower, Professor Duane S. Boning, Michael B. McIlrath

5 M. McIlrath, D.S. Boning, and D.E. Troxel, "Architecture for Distributed Design and Fabrication," *Proc. SPIE* 2913: 134-47 (1997).

We have developed a distributed control system architecture and implemented a software/hardware prototype for the run-by-run control of plasma etching.[6] The modular controller architecture includes sensor communication and analysis; controller communication and execution; equipment communication and recipe download; and user interface. Currently, we are working on the application of this architecture to epitaxial silicon fabrication. The goal of this work, undertaken in conjunction with On-Line Technologies and Applied Materials, is to develop cell controller software which will obtain data from in-line resistivity and thickness sensors, analyze the data to determine drifts in the epitaxial film process, and modify and download new process recipes to the fabrication tool.

3.2.4 Semiconductor Process Repository

Project Staff

Matthew D. Verminski, William P. Moyne, Michael B. McIlrath, Professor Donald E. Troxel

We have developed the core of a software system to facilitate distributed process research and design. This core capability allows users to retrieve and examine process flows from multiple process libraries across the network.

A distributed process repository interface has been developed. The repository application programming interface (API) is encapsulated by an OMG CORBA distributed object model and defined by an interface description language (IDL) specification. The process object model used to encapsulate the process repository API is based on the semiconductor process representation (SPR) information model. The IDL specification is programming language-neutral; application clients and repository services may be implemented in any language supported by a CORBA-compliant object request broker (ORB) and interoperate across a local or wide-area network. Process repositories may be distributed; process objects and services may be located at various sites transparently to application clients. Applications and services may interoperate using entirely distinct ORB implementations if a common protocol such as the internet interORB protocol (IIOP) or appropriate bridges are available.

The present SPR IDL development includes the base information model. This standard process representation interface provides a common facility to communicate fabrication processes. The fabrication process information organizes processes into smaller subprocesses. At each level, the process can be described from different views. These include the *effect* of a process on the wafer, the *environment* around the wafer during the process, and the *equipment* settings during the process. Each view contains parameters that describe some aspect of the wafer, environment, or equipment during some interval of time. Dynamic attributes (property lists) are also supported for maximum extensibility. The base SPR IDL has been extended to include specific effects and parameters with statistical information.

A distributed software architecture for semiconductor process design has been defined and implemented in Java with the OrbixWeb ORB. The implementation communicates with any ORB adhering to the IIOP. A persistent storage mechanism has been implemented using the object design objectstore persistent storage engine (PSE) for Java.

Other services to manage, query and find distributed objects are being developed. Their interfaces are based upon the OMG CORBA services specifications. A life cycle service for creating, deleting, copying, and moving distributed objects has been developed. A query service and a trader service have also been implemented. Together, the services provide essential capabilities for the development of distributed and shared applications for semiconductor process research and design.

Thesis

Verminski, M. *A Distributed Software Architecture for Semiconductor Process Design.* S.M. thesis. Department of Electrical Engineering and Computer Science, MIT, February 1998.

6 A. Gower, D. Boning, and M. McIlrath, “Flexible, Distributed Architecture for Semiconductor Process Control and Experimentation,” *Proc. SPIE* 2912: 146-58 (1997).

3.2.5 Exploring Semiconductor Device Parameter Space using Rapid Analytical Modeling

Project Staff

Brian Lee, Michael B. McIlrath, Professor Duane S. Boning, Professor Donald E. Troxel, Professor Anantha P. Chandrakasan

One of the most important decisions a circuit designer must make is the selection of a specific device structure which is to be used within a given circuit design. To find desirable device characteristics, a designer must often revert to potentially time consuming techniques and calculations (e.g., numerical device simulators such as MEDICI). In this project, a software tool has been developed and implemented in Java which allows a designer to explore rapidly the device parameter space for a given technology, as well as across different technologies (see Figure 1). The technique of exploring parameter space utilizes a method of rapid analytical modeling to allow for faster, but less accurate, evaluations than one might get through established methods of numerical simulation tools such as MEDICI or PISCES, offering an alternative to such simulators for circuit designers who wish to have rough estimates of parameter variation information, or device structure feasibility.

In general, any semiconductor device can be defined as a device model. Device models are sets of equations which serve to define the current-voltage characteristics of a particular device as a function of several parameters, some of which may represent environmental effects on a device (such as temperature), physical properties of the device (such as channel width), or fitting parameters (such as the channel length modulation parameter). These parameters and the sets of their feasible values form a parameter space which can be thought of as the set of all possible combinations of semiconductor device parameter values.

The idea of semiconductor device parameter space exploration is to examine the subset, or space, of semiconductor parameters under defined electrical constraints and to determine a method of describing and utilizing the subsets to provide useful information. Specifically, the object of the tool is to determine the feasible parameter space of a specific device model given user-defined electrical and parameter constraints.

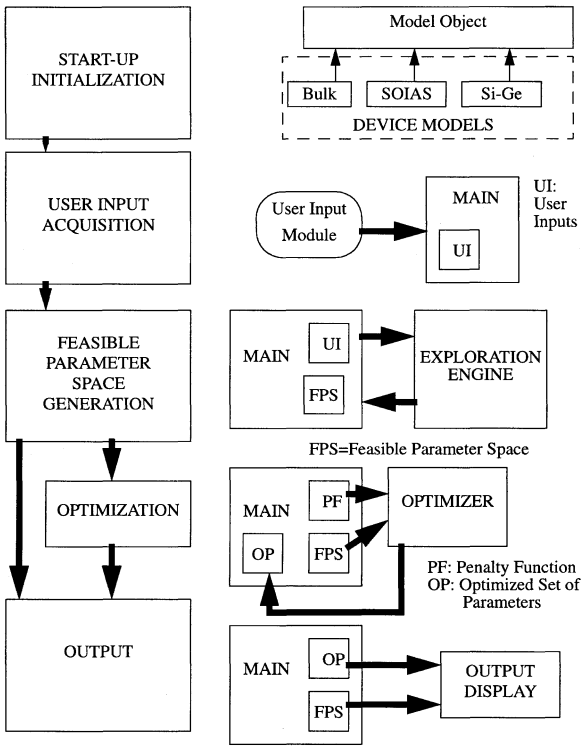

Figure 1. Operational flow of design space exploration tool.

Given a device model which defines a current-voltage relationship as a function of a vector of semiconductor device parameters and a voltage vector, there exists a parameter space of all physical parameters of a device. In general, this vector can be thought of as a set of voltages applied to the terminals of a device. The goal of exploring parameter space is to find a region within the space of all physical parameters where the parameter values of every point within the region meet some specific electrical criteria.

Thesis

Lee, B. *Exploring Semiconductor Device Parameter Space using Rapid Analytical Modeling.* S.M. thesis. Department of Electrical Engineering and Computer Science, MIT, January 1998

3.3 Helium Breath: An Updated Course 6.111 Curriculum

Project Staff

Marc D. Tanner, Professor Donald E. Troxel

Helium Breath is a challenging laboratory assignment which gives students practical experience designing and building a complex digital system. In addition, the assignment is designed to be fun and appealing to a wide range of students. It is intended to replace and update an assignment previously used in course 6.111 Introductory Digital Systems Laboratory, MIT's digital design course. Helium Breath emphasizes several important concepts used in digital systems. Moreover, it gives students hands-on experience with complex programmable logic technology which is standard in industry; this technology was previously not covered in any undergraduate course at MIT.

The assignment requires students to build a pitch shifter for audio signals. The system takes as input an audio signal and scales it up or down in pitch without changing the time-base of the signal. The sampling rate is the same for both the input and output signals; the system works in real time, with only a slight delay between input and output. The name “Helium Breath” evokes memories of breathing in the helium from a balloon and then speaking in an absurdly-high voice, and this is one of the effects that can be demonstrated with the completed system.

Thesis

Tanner, M.D., *Helium Breath: An Updated 6.111 Curriculum.* M. Eng. thesis. Department of Electrical Engineering and Computer Science, MIT, May 1998.