Focused Research Center for Gigascale Integration

Academic and Research Staff
Professor Carl V. Thompson
Professor Donald E. Troxel

Graduate Students
Syed M. Alam
Yonald Chery

Technical and Support Staff
Francis M. Doughty

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1. Focused Research Center for Gigascale Integration

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Project Staff
Syed M. Alam, Yonald Chery, Stefan P. Hau-Riege, Carl V. Thompson, Donald E. Troxel

1.1 Software Tools for Process-Sensitive Reliability Assessments of IC Designs (ICS)

Integrated circuits are currently designed using simple and conservative 'design rules' to ensure that the resulting circuits will meet reliability goals. This simplicity and conservatism leads to reduced performance for a given circuit and metallization technology. We are developing a TCAD tool, ERNI, which will allow process-sensitive and layout-specific reliability estimates for fully laid out or partially laid out integrated circuits (see Figure 1).

Circuit-level reliability analyses require the assessment of the reliability of a large number of sometimes complexly connected interconnect trees. An interconnect tree is a continuously connected high conductivity metal, within one layer of metallization, bound by contacts or vias filled with diffusion barriers. We have shown through modeling and experiments that the resistance saturation observed in straight via-to-via lines, which can lead to immunity from electromigration-induced failure, also occurs in more complex interconnect trees. We have also shown that trees will be 'immortal' if their effective current-density line-length product, $(\mathrm{jL})_{eff}$, is below a critical value. This effective jL product is defined as the maximum value of the sums of the jL products in individual lines taken over all the possible paths through a tree. The jL product that defines immortality can be determined from

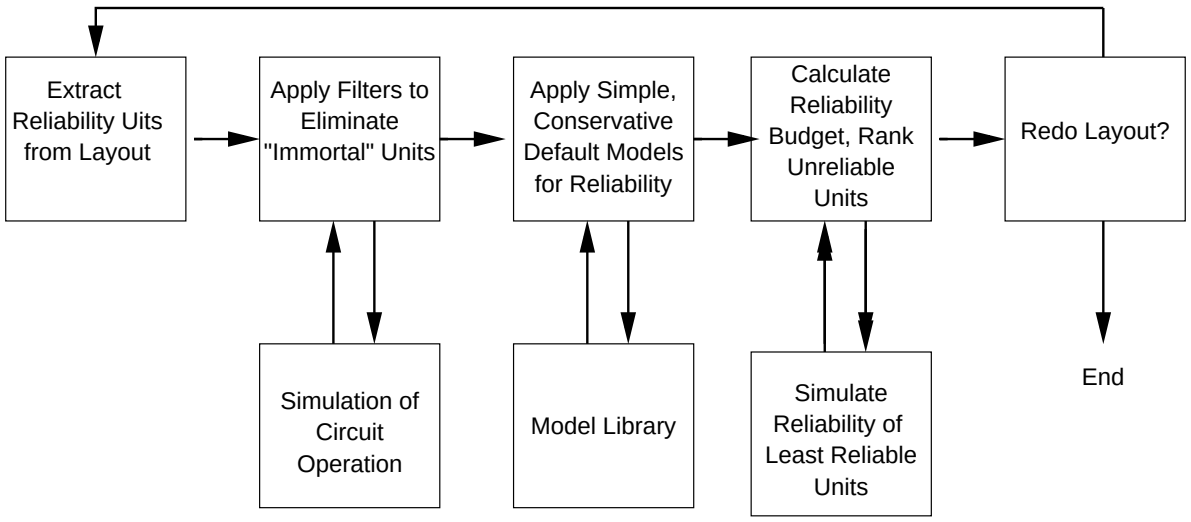

Figure 1: A flow chart for a full hierarchical circuit-level reliability assessment, the basis for the prototype tool ERNI.

experimental characterization or simulation of the reliability of straight via-to-via lines.

Simple tests for tree immortality can be used in a hierarchical way to eliminate trees from further more computationally intensive reliability assessments. We have carried out a first-level analysis on microprocessor layouts available on the web, and found that at service conditions the majority of interconnect trees are immortal, even when the worst-case assumption is made that all the limbs of all the trees are at the maximum current density. Filtering of immortal trees significantly reduces the computations required for circuit-level reliability assessments.

After filtering of immortal trees, the reliability of mortal trees must be assessed. This can be done through simulations of the reliability of individual trees, but this computationally intensive method should be reserved for the most problematic trees, those with the least reliability, and which are least convenient to 'fix' through layout modifications. We have suggested computationally simple and conservative 'default' models for assessment of tree reliabilities based on the Korhonen analysis and have tested models and simulations through experiments on simple interconnect trees. Our experimental results are consistent with both our analytic models and simulations. With the default models, a first prototype of ERNI has been developed.

We are now developing a version of ERNI, ERNI-3D, which can be used for analysis of the reliability of three dimensional circuits made through bonding of two or more device layers. We have already developed layout methodologies for 3D Integrated Circuits and extended Magic, a widely used layout editor in the academia, to 3DMagic for designing 3D test circuits. A 3D 8-bit adder has been designed as a simple test circuit for ERNI-3D. Moreover, using 3DMagic several students have designed 3D FPGA for performance comparison with its 2D counterpart. Such analysis has shown performance improvement in terms of signal delay, power consumption and resource utilization in the 3D circuit.