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1.1 Software Tools for Process-Sensitive Reliability Assessments of IC Designs (ICS)

Integrated circuits are currently designed using simple and conservative 'design rules' to ensure that the resulting circuits will meet reliability goals. This simplicity and conservatism leads to reduced performance for a given circuit and metallization technology. We have developed a TCAD tool, ERNI, which will allow process-sensitive and layout-specific reliability estimates for fully laid out or partially laid out integrated circuits (see Figure 1).

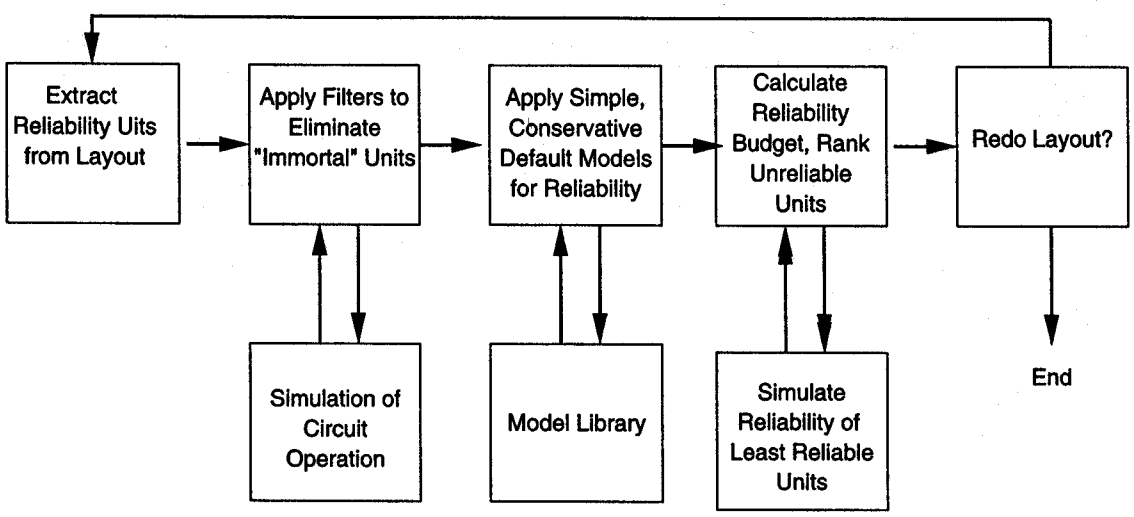

Figure 1: A flow chart for a full hierarchical circuit-level reliability assessment, the basis for the tool ERNI.

Circuit-level reliability analyses require the assessment of the reliability of a large number of sometimes complexly connected interconnect trees. An interconnect tree is a continuously connected high conductivity metal, within one layer of metallization, bound by contacts or vias filled with diffusion barriers. We have shown through modeling and experiments that the resistance saturation observed in straight via-to-via lines, which can lead to immunity from electromigration-induced failure, also occurs in more complex interconnect

trees. We have also shown that trees will be 'immortal' if their effective current-density line-length product, $(jL)_{eff}$, is below a critical value. This effective jL product is defined as the maximum value of the sums of the jL products in individual lines taken over all the possible paths through a tree. The jL product that defines immortality can be determined from experimental characterization or simulation of the reliability of straight via-to-via lines.

Simple tests for tree immortality are used in a hierarchical way to eliminate trees from further more computationally intensive reliability assessments. We have carried out a first-level analysis on microprocessor layouts available on the web, and found that at service conditions the majority of interconnect trees are immortal, even when the worst-case assumption is made that all the limbs of all the trees are at the maximum current density. Filtering of immortal trees significantly reduces the computations required for circuit-level reliability assessments.

After filtering of immortal trees, the reliability of mortal trees is assessed. This can be done through simulations of the reliability of individual trees, but this computationally intensive method is reserved for the most problematic trees, those with the least reliability, and which are least convenient to 'fix' through layout modifications. We have computationally simple and conservative 'default' models for assessment of tree reliabilities based on the Korhonen analysis. We have tested models and simulations through experiments on simple interconnect trees. Our experimental results are consistent with both our analytic models and simulations. With the default models, a first version of ERNI has been developed.

Recent development in semiconductor processing technology has enabled the fabrication of a single integrated circuit (IC) with multiple device-interconnect layers or wafers stacked on each other. This approach is commonly referred as the 3D integration of ICs. Although there has been significant research on the impact of 3D integration on chip size, interconnect delay, and overall system performance, the reliability issues in the 3D interconnect arrays are fairly unknown. In this research, a novel Reliability Computer Aided Design (RCAD) tool, ERNI-3D, for the reliability analysis of interconnects in a 3D IC has been developed. Using this tool, circuit designers can get interactive feedback on the reliability of their circuits associated with electro-migration, 3D bonding, and joule heating. Based on a joint probability distribution, a full-chip reliability model combines all the reliability figures of different components to give a useful number for designers' reference. This initial version of ERNI-3D treats 3D circuits with two wafers or device-interconnect layers in the stack. However, the data-structures and algorithms in the tool are generic enough to make it compatible with 3D circuits with more than two device-interconnect layers and also incorporate more sophisticated reliability models in the future. Since the 3D integration technology is not yet widespread, and no CAD tool supports IC layouts for such technology, a novel layout methodology has been implemented in MAGIC, a widely used layout editor in academia. Apart from the CAD tool works, this research has also led into development and interesting experiments with some 3D test circuits. The test circuits investigated are a 3D 8-bit adder and 3D field-programmable gate array (FPGA).