Power Aware Circuits and Systems for Wireless Applications

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1. Ultra-Wideband Radio Transceivers

Sponsors
This work is sponsored by Hewlett-Packard through the HP-MIT Alliance, DARPA, and the Air Force Research Laboratory under agreement number F33615-02-2-4005.

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Ultra-wideband (UWB) radio is a new wireless technology that was recently approved for commercial use by the Federal Communications Commission. Depending on the application, it utilizes bandwidth from DC to 960MHz, or 3.1 to 10.6GHz. Contrary to traditional narrowband, single-tone radio signals, a UWB signal is typically composed of a pulse train of sub-nanosecond pulses modulated either in polarity or position as shown in Figure 1. The narrowness of the pulses in time corresponds to a wide bandwidth in the frequency domain. Since the total power is spread over such a wide swath of frequencies, its power spectral density is extremely low. This minimizes the interference caused to existing services that already use the same spectrum. On account of the large bandwidth used, UWB links are capable of transmitting data over tens of megabits per second. Other benefits include low probability of interference and detection, and precise positioning capability.

Figure 1 : Transmitting Information in a UWB System

There are many design challenges that need to be overcome in order to realize UWB radio systems in a small form-factor. The most pressing is antenna design. Successful transmission and reception of a UWB pulse that occupies a GHz or more of spectrum requires an antenna that has low dispersion and VSWR throughout the entire band. Typical wideband antennas such as horns, helices and bicones are incompatible with integrated circuits, which require electrically small antennas such as dipoles, monopoles or planar antennas. Planar antennas, while generally designed to be resonant, can be designed for a degree of frequency independence by exponentially increasing the distance between the radiating planar element and its ground plane. We will be researching novel antenna structures, and will try to apply analogous practical insights from narrowband antenna design to UWB.

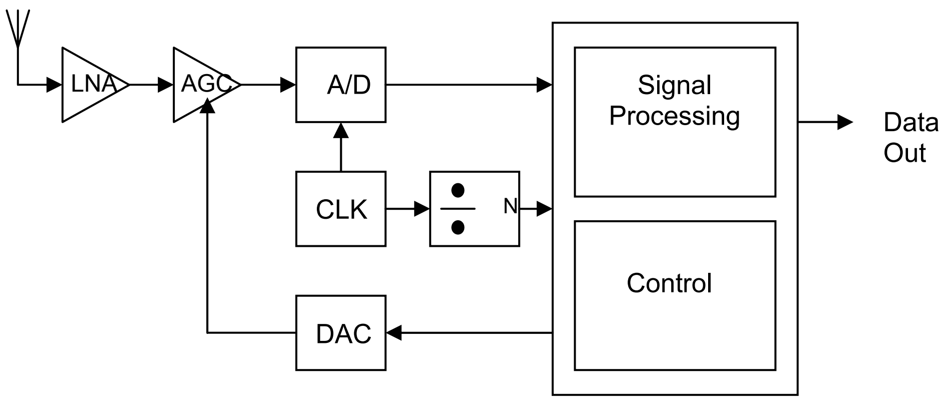

Fig. 2 : Digital Architecture for Baseband UWB Receiver

In our efforts to develop a fully-integrated UWB transceiver, we have begun by exploring an all-digital architecture for baseband UWB, where the frequency content of the transmitted pulse train is contained in 15MHz-960MHz bandwidth. In this architecture, the signal received at the antenna is amplified and immediately digitized as shown in Fig. 2. All the processing for extracting the received signal from noise, detecting, and demodulating is done in the digital domain. A front-end chip for this architecture has been designed, and the layout of the chip is shown in figure 3. The front-end amplifier provides 34dB of gain over the bandwidth of interest. The analog to digital converter is a time-interleaved ADC that provides 4 Gigasamples/sec with 4 bits of resolution over a 500mV input voltage range. This chip was fabricated in Dec 2002 in a 0.18μm TSMC mixed-mode process and is currently being tested. Work is underway for a second chip, a complete ultra-wideband RAKE receiver that performs coarse and fine acquisition, and data demodulation. This chip will be fabricated in April of 2003.

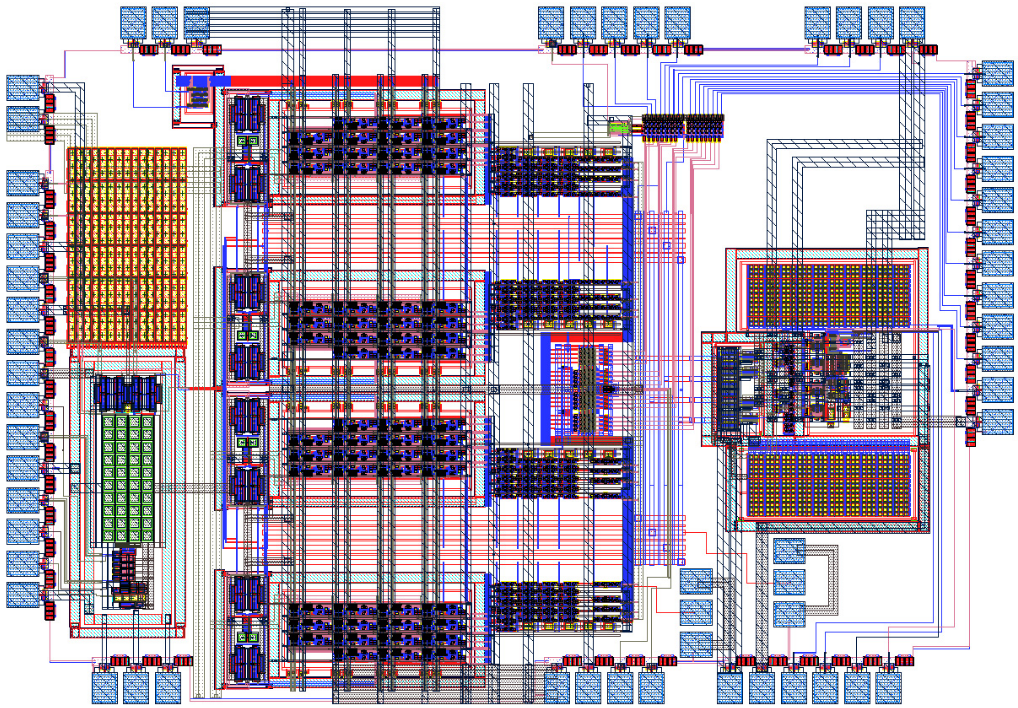

Fig. 3: Baseband UWB Receiver Front-End

Our next target is the 3.1 to 10.6 GHz band that the FCC has allocated for communications applications. This large allocated bandwidth may be utilized as a monolithic block (uni-band), or broken up into adjacent sub-bands (multi-band). The choice of a uni-band or multi-band approach will have significant ramifications on system design, power consumption, area, cost and programmability. The goal of our research is to analyze these trade-offs in order to determine a suitable architecture for our next-generation UWB transceiver.

2. µAMPS: Power Aware Wireless Sensor Networks

Sponsors

This research is sponsored by the Defense Advanced Research Project Agency (DARPA) Power Aware Computing/Communication Program and the Air Force Research Laboratory, Air Force Materiel Command, USAF, under agreement number F30602-00-2-0551; by the Army Research Laboratory (ARL) Collaborative Technology Alliance, through BAE Systems, Inc. subcontract RK7854; and by Hewlett-Packard under the HP/MIT Alliance. Julia Cline is supported by an SRC Masters' Scholarship. Rex Min is supported by an NDSEG Fellowship. Alice Wang is supported by an Intel Fellowship.

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The idea of wireless microsensor networks has garnered a great deal of attention and interest. A distributed wireless microsensor network consists of hundreds to several thousands of small sensor nodes scattered throughout an area of interest. Each node individually monitors its environment and collects data as directed by the user, while the network collaborates as a whole to deliver high-quality observations to a central base station. The fusion of observations from different perspectives offers a high-resolution, multi-dimensional picture of the environment that is not possible with fewer sensors. The sheer number of nodes naturally leads to the network's fault-tolerance and robustness to the loss of individual nodes, making maintenance unnecessary. Nodes can be deployed simply by scattering them about the region of interest or dropping them by air; the nodes can organize themselves into networks without user intervention. These advantages, as well as the nodes' small size, make sensor networks ideal for any number of inhospitable or inaccessible locations where deployment is difficult, wires impractical, and maintenance impossible.

The energy consumption and lifetime requirements are quite possibly the greatest challenge to the design of efficient microsensor networks. Replacing the batteries of thousands of nodes in a hostile or inaccessible environment is simply not possible; nodes must be designed to operate without maintenance for years from a tiny on-board battery. To achieve these goals, we have
Our approach to meeting these lifetime requirements is to provide energy-agile fabrics, where hardware and software knobs allow for system level energy-efficiency while still achieving the desired quality of service and latency. We have developed a system-level power aware design methodology that allows for optimization at all levels of design ranging from communication protocols and OS-directed power management, to scalable algorithms, architectures and circuits. A system with a multitude of hardware and software knobs provides the end-user a high degree of freedom for optimal energy-management across a variety of operating scenarios.

We have designed and fabricated uAMPS-1, a compact wireless microsensor node that demonstrates advanced power aware concepts. Based on the StrongARM-1110, uAMPS-1 integrates dynamic voltage scheduling, hardware and software support for various shutdown modes, a fully flexible link layer protocol, and fine-grained energy-agile radio output power control. Dynamic voltage scheduling reduces processor energy by a factor of three (including regulator overhead) for realistic workloads when compared to a conventional fixed 1.5V system. In addition to processor dynamic voltage scaling, additional power saving modes can individually shut down the acoustic sensor and analog circuitry, the transmit or receive paths of the radio, and

the entire radio (including the digital baseband circuitry), with provisions made for any peripherals that may be added to the node in the future. A new link manager interface allows the processor to manage the power consumption of the radio, baseband, and MAC functional units. Energy scalable communication is enabled through hardware hooks that include variable output transmit power, PLL closed-loop and open-loop modes, energy-agile ECC, and variable packet size. Variable output transmit power is implemented with a power amplifier whose output power is adjustable between 0dBm and 20dBm. A basestation interface board has been designed to augment the standard node with PC connectors (RS-232, USB) and an AC power supply, thereby transforming the standard node into a basestation.

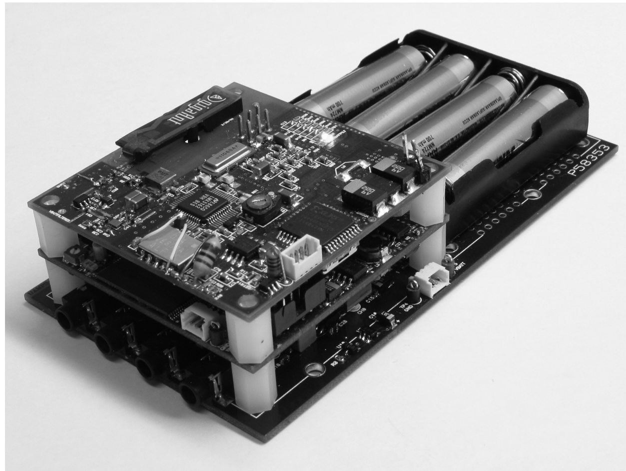

Figure 1. uAMPS-1 microsensor node.

The node has been an instrumental tool for advancing our understanding of the physical nature of wireless sensors. We have utilized the node to validate energy and performance models, to characterize the operating and power consumption characteristics of software running on a processor, to test the limits of communication performance, and to parameterize large-scale simulations of nodes communicating in a network. Specifically, we have measured an order of magnitude variation in energy consumption is possible across the discrete operational modes of the uAMPS-1 node. The following canonical modes of operation have been identified:

- *Deep sleep:* all systems powered off. A time wakes the processor after a preprogrammed amount of time (50mW)
- *Threshold detection:* Only the sensor is powered. Detection of a sufficiently strong acoustic signal will wake the node (65mW)
- *Sensing:* Sensor and processor active for data collection (150-700mW)
- *Receiving:* Processor and radio receiver active (500-1000mW)
- *Transmitting:* Processor and radio transmitter active (300-1900mW)

Hardware and software hooks provide a range of shutdown modes that, through the OS, demonstrate 8X scaling in processor power, 6X in transmitter power, and 40X overall.

The uAMPS-1 node has been demonstrated in two real-world settings. In April 2002 at the Aberdeen Proving Grounds in Maryland, we demonstrated three-channel acoustic sensing using the uAMPS-1 node and collected acoustic data of more than 10 tracked wheeled vehicles. Three microphones were connected to a single uAMPS node by means of a new multi-channel acoustic sensor board that was added to the node. The data recorded has been analyzed using ARL and ISI beamforming algorithms. In May 2002, we demonstrated an end-to-end beamforming application using the uAMPS-1 node prototype. One sensor node samples acoustic data from three microphones and performs the beamforming computation locally before transmitting the estimated LOB of the acoustic source to the basestation node. The basestation node, a derivative of the uAMPS-1 node, reports the updated position of the acoustic source to a PC running a Java application. This complete system demonstration verifies the integrity of the sensor (A/D), processor, radio, and two-way communication link running over a protocol stack with TDMA.

In the course of developing these demonstrations, we have developed an energy efficient implementation of algorithms for target tracking and Line of Bearing estimation. The baseline algorithms from ARL implement local FFT and frequency domain delay-and-sum beamforming for clusters of microphone arrays. By partitioning the computation of LOB estimation across the cluster such that some computation is performed in parallel, the supply voltage and frequency of individual nodes are reduced. Optimal partitioning policies have been drived, and energy savings of 2X have been reported through optimal system partitiong.

In addition to the development of the uAMPS-1 hardware, we have considered routing and data dissemination protocols for wireless sensor networks. We have derived and proved the existence of a minimum-energy transmission distance for a wireless communication ("characteristic distance") and applied this knowledge to improve the energy efficiency of multihop routing protocols for wireless networks. Equidistant hops over the characteristic distance has been proved as the optimal multi-hop data relay policy. For typical COTS-based sensor nodes, the characteristic distance is about 20 meters. A dithering relay policy for a generic sensor array was developed to approach the energy-efficiency of the optimal multi-hop policy; the nodes chosen for the relay path are alternated such that the average transmission distance is close to the characteristic distance.

An Address-Free Forwarding protocol to forward sensor data to a base station in an environment where radio receivers may shut down frequently and arbitrarily to conserve network energy, and developed a companion simulation tool for high-density networks. In Address-Free Forwarding, sensor nodes obtain a metric of their distance to the base station, and packets are forwarded dynamically based upon receiving nodes' distance to the base station rather than a specific address. The protocol has been developed and evaluated using a companion simulation tool.
This Java-based tool enables effortless, rapid simulations of thousand-node wireless networks, with real-time, graphical output.

To encourage the use of uAMPS-1's power aware capabilities in application software, we have introduced a power aware API that bridges the gap between low-level settings (e.g. processor voltage and transmit power) and performance parameters more relevant to an application (e.g. latency and reliabliity). The integrated power-aware communication API permits the user to define bounds for the performance of a given application, and the API converts these bounded, application-level constraints into the least-energy parameter settings for energy-scalable hardware. This allows for a user-friendly and graceful exchange between performance and energy savings.

Our goal for the upcoming uAMPS-2 hardware is to design a highly integrated, yet flexible, sensor node based on two dedicated chips. One chip contains all the analog and RF parts of the radio, while the other one implements all digital functionality. To serve as a proof of concept and early real-time validation, we first target an FPGA implementation that will interface with the radio of the µAMPS-1 project.

The uAMPS-2 node will be composed of the following subsystems:

- Energy-scalable micro-power DSP at 10 MIPS provides an energy-efficient alternative to a complete general-purpose processor
- Dedicated hardware accelerator support the DSP, aggressively trading off energy versus performance.
- A protocol processor dedicated to packet handling functions that supports efficient communication power management functionalities
- A radio that provides several control hooks for power-awareness and is flexible enough to scale the transmit rate from virtual zero to 1 Mbps, with a range from 10 m to 1 km.

Our overall power consumption target is 100 uW, excluding the power amplifier. This aggressive design pushes the envelope in power aware, reconfigurable system design, and will necessitate additional innovations in architectures and techniques across the system hierarchy.

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