Focused Research Center for Gigascale Integration

Academic and Research Staff
Professor Carl V. Thompson, Professor Donald E. Troxel

Graduate Students
Syed M. Alam, Yonald Chery

Technical and Support Staff
Francis M. Doughty

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Project Staff
Syed M. Alam, Yonald Chery, Carl V. Thompson, Donald E. Troxel

Software Tools for Process-Sensitive Reliability Assessments of IC Designs (ICS)
Integrated circuits are currently designed using simple and conservative `design rules' to ensure that the resulting circuits will meet reliability goals. This simplicity and conservatism leads to reduced performance for a given circuit and metallization technology. We have developed a TCAD tool, ERNI, which will allow process-sensitive and layout-specific reliability estimates for fully laid out or partially laid out integrated circuits (see Figure 1).

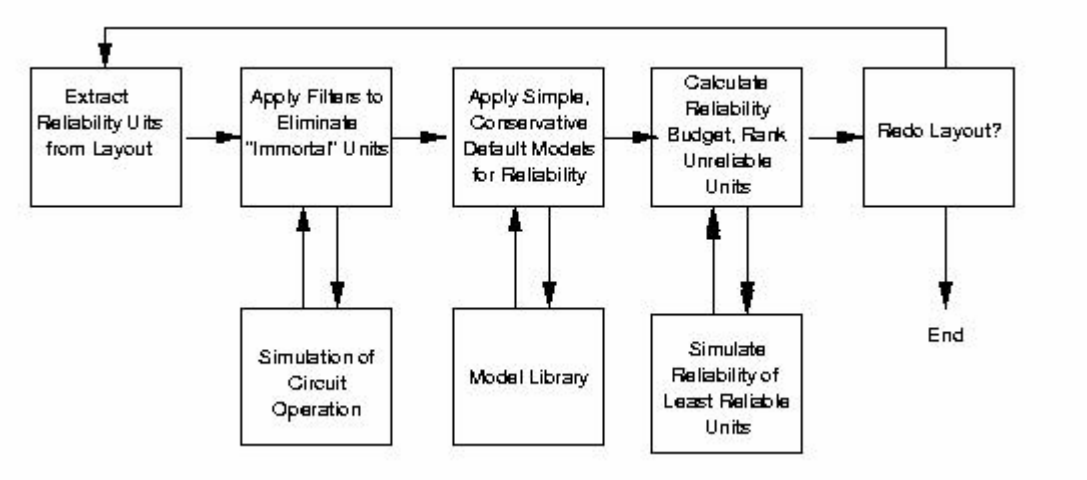

Figure 1: A flow chart for a full hierarchical circuit-level reliability assessment, the basis for the tool ERNI.

Circuit-level reliability analyses require the assessment of the reliability of a large number of sometimes complexly connected interconnect trees. An interconnect tree is a continuously connected high conductivity metal, within one layer of metallization, bound by contacts or vias filled with diffusion barriers. We have shown through modeling and experiments that the resistance saturation observed in

straight via-to-via lines, which can lead to immunity from electromigration-induced failure, also occurs in more complex interconnect trees. We have also shown that trees will be `immortal' if their effective current-density line-length product, (jL)$_{eff}$, is below a critical value. This effective jL product is defined as the maximum value of the sums of the jL products in individual lines taken over all the possible paths through a tree. The jL product that defines immortality can be determined from experimental characterization or simulation of the reliability of straight via-to-via lines.

Simple tests for tree immortality are used in a hierarchical way to eliminate trees from further more computationally intensive reliability assessments. We have carried out a first-level analysis on microprocessor layouts available on the web, and found that at service conditions the majority of interconnect trees are immortal, even when the worst-case assumption is made that all the limbs of all the trees are at the maximum current density. Filtering of immortal trees significantly reduces the computations required for circuit-level reliability assessments.

After filtering of immortal trees, the reliability of mortal trees is assessed. This can be done through simulations of the reliability of individual trees, but this computationally intensive method is reserved for the most problematic trees, those with the least reliability, and which are least convenient to `fix' through layout modifications. We have computationally simple and conservative `default' models for assessment of tree reliabilities based on the Korhonen analysis. We have tested models and simulations through experiments on simple interconnect trees. Our experimental results are consistent with both our analytic models and simulations. With the default models, a first version of ERNI has been developed.

Recent development in semiconductor processing technology has enabled the fabrication of a single integrated circuit with multiple device-interconnect layers or wafers stacked on each other. This approach is commonly referred to as the Three-Dimensional or 3D integration of ICs. Although there has been some research on the impact of 3D integration on chip size, interconnect delay, and overall system performance, the reliability issues in the 3D interconnect arrays are fairly unknown. We have extended the reliability concepts in ERNI and developed a framework for reliability analysis in 3D circuits with a novel Reliability Computer Aided Design (RCAD) tool, ERNI-3D. Using ERNI-3D, circuit designers can get interactive feedback on the reliability of their circuits associated with electromigration, 3D bonding, and joule heating.

As the 3D integration technology is not yet widespread, and no CAD tool supports IC layouts for such a technology, we first developed a comprehensive 3D circuit layout methodology. The circuit on each wafer or device interconnect layer can be laid out separately with inter-wafer via information embedded in the layout. The inter-wafer via information is generalized into three categories sufficient for defining all types of interconnection between wafers in a 3D stack (see Figure 2). A strategy for layout-file management that incorporates the orientation of each wafer in the bonding process is also proposed. We have implemented the layout methodology in 3D-MAGIC, an extension of MAGIC originally developed at UC Berkeley and widely used in academia. The test circuits designed with 3D-MAGIC are a 3D 8-bit adder and an 8-bit encryption processor mapped into a 3D FPGA.

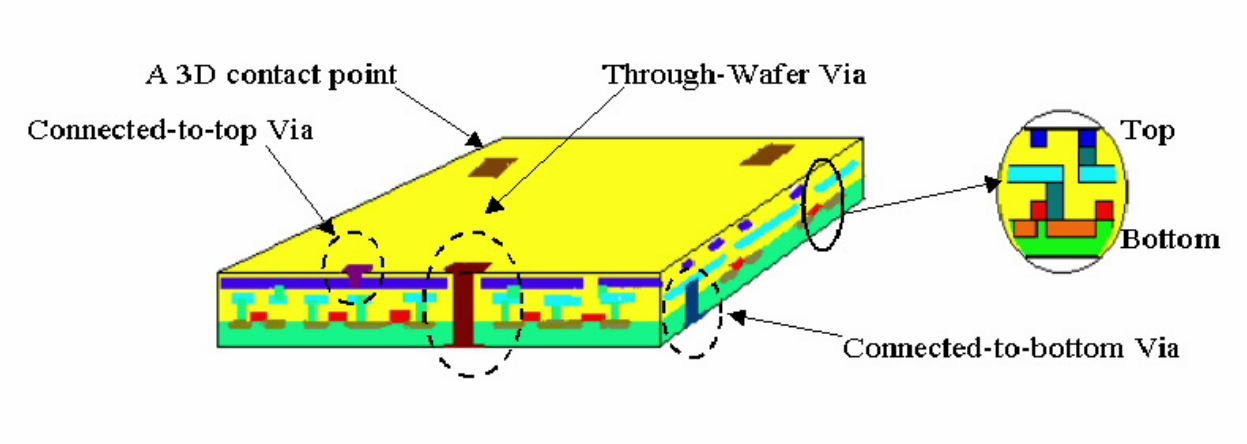

Figure 2: Different types of via/contact for 3D ICs.}

The reliability CAD tool, ERNI-3D, parses 3D circuit layouts and extracts both conventional and 3D interconnect trees. It employs the Hierarchical Reliability Analysis approach, and filters out a group of immortal trees using their current-density length products. After the filtering process, the stringent reliability models are applied to the remaining interconnect trees for computing their median and mean time to failures. Finally, all the different time to failures are combined using a joint probability distribution to report a single reliability figure for the whole chip. This initial version of ERNI-3D treats 3D circuits with two wafers or device-interconnect layers in the stack (see Figure 3). However, the data-structures and algorithms in the tool are generic enough to make it compatible with 3D circuits with more than two device- interconnect layers and to allow the incorporation of more sophisticated reliability models in the future.

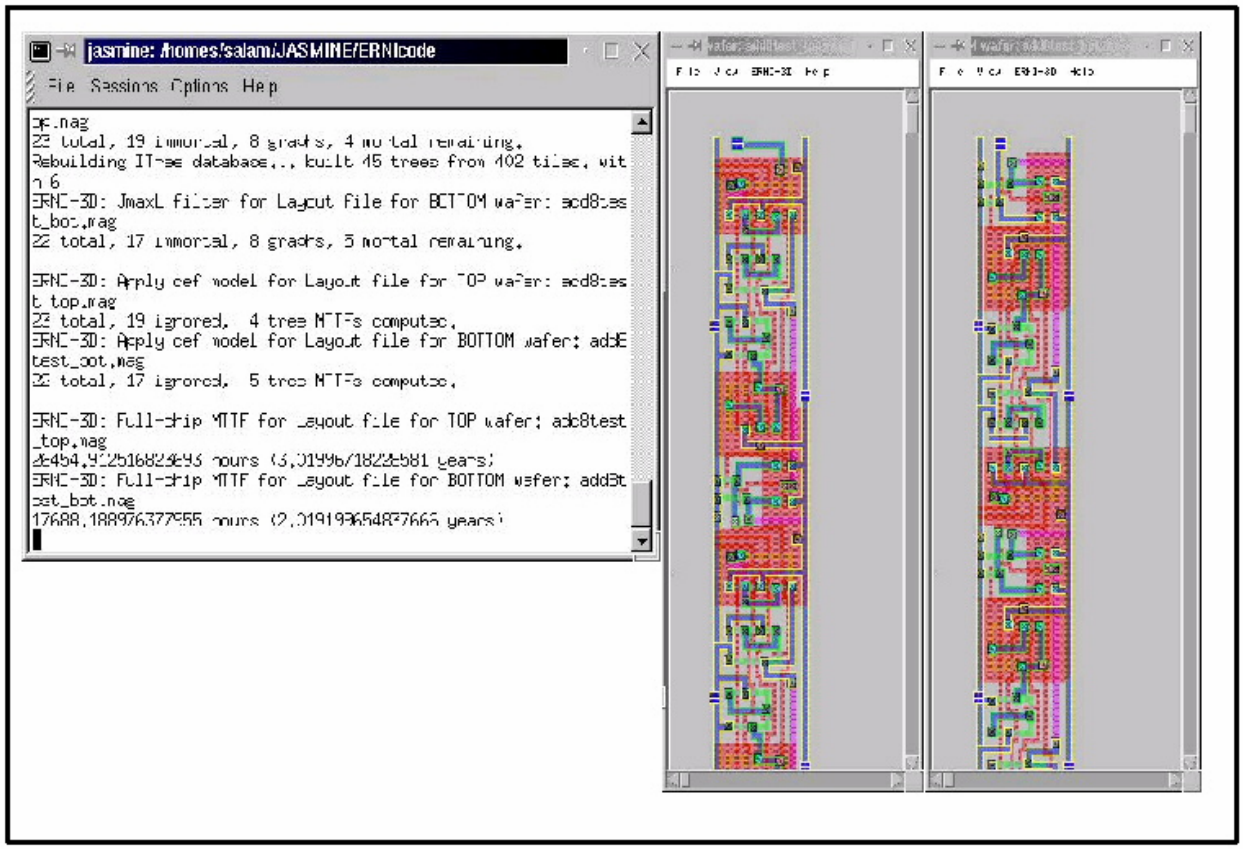

Figure 3: Graphical User Interface of ERNI-3D. Here ERNI-3D is run on a 2-wafer 3D 8-bit Adder layout.