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A PCI/PCI-X Test Card for I/O System Verification

As I/O systems become large and more complex, thge task to validate a system with one or more newly designed bridge components becomes increasingly challenging. In current industry standard I/O system verification, there exists a detrimental absence of a connection between the t est enviroments of presilicon software simulations and postsilicon hardware diagnostic testing. Verification engineers are currently using disparate, adhoc methods of building system environments for software tests and hardware tests. This makes it difficult to recreate hardware bugs in simulation or to run realistic system tests before the hardware is manufactured. A synthesizable dual-mode PCI/PCI-X card has been developed to be used in both presilicon and postsilicon verfication stages of a server I/O system with a newly developed PCI/PCI-X bridge ASIC. This test card has been successfully tested for functionality and timing requirements. The test card has enabled common system platform development for hardware bring-up and testing as well as system software simulations.

6.111 Gate Array PC Board

Currently, MIT course 6.111 is taught using the aid of a circuit board connected to each students lab kit, with each circuit board mounting several Complex Programmable Logic Devices (CPLDs). Each of these devices can be programmed using VHDL to simulate larger and more complex digital systems than would be possible for a student to wire on the breadboards of the lab kit alone.

The MIT 6.111 Gate Array PC Board is a further refinement of the original 6.111 CPLD PC Boards. Instead of using four CPLDs, these boards will use a pair of Field Programmable Gate Arrays (FPGAs). Th FPGAs will be programmable using VHDL, and have been chosen to counteract a number of common problems students dealt with when using the CPLD boards: the number of accessible I/O pins, the ability to assign signals to pins freely, the size and complexity of digital logic capable of being simulated, and the accessibility of programming resources in the 6.111 laboratory.

Presentations

Syed M. Alam, Donald E. Troxel, and Carl V. Thompson, “ERNI-3D: Reliablity of 3-D Integrated Circuits, poster presention at the Interconnect Focus Center 3rd Annual Review," Atlanta, Georgia,
January 7, 2002 and M. I. T Interconnect Focus Center Workshop, Cambridge, Massachusetts, March 22, 2002.

Syed M. Alam, Donald E. Troxel, and Carl V. Thompson, “Development of Tool Suite for 3-D Integrated Circuits," poster presented at the Interconnect Focus Center 4th Annual Review, Atlanta, Georgia, October 7-8, 2002

Publications

S. Alam, D. Troxel, and C. Thompson, "A Comprehensive Layout Methodology and Layout-specific Circuit Analyses for Three-dimensional Integrated Circuits," in Proceedings of International Symposium on Quality Electronic Design, pp. 246-251, March 2002.

Accepted for Publication

Cho, W., Sachs, E.M., Patrikalakis, N.M., and Troxel, D.E., “A Dithering Algorithm for Local Composition Control with Three-Dimensional Printing", accepted, Computer-Aided Design, forthcoming.

Proceedings of Refereed Conferences

Alam, S.M., Troxel, D.E., and Thompson, C.V., “Layout-Specific Circuit Evaluation in 3-D Integrated Circuits", Proceedings of International Symposium on Quality Electronics Design (ISQED-02), San Jose, California, March 18-20, 2002.

Invited Lectures

C.V. Thompson, R. Tedepalli, S. Alam, D.E. Troxel, “Reliability of 3D Integrated Circuits," MARCO Interconnect Focus Center Quarterly Workshop, MIT, Cambridge, March 22, 2002.

Theses

Amy K. Mitby, “A PCI/PCI-X Test Card for I/O System Verification," M. Eng., Department of Electrical Engineering and Computer Science, M.I.T., February 2002.

Brian M. Perrin, “6.111 Gate Array PC Board, M. Eng., Department of Electrical Engineering and Computer Science, M.I.T., June 2002.