Circuit and System Level Tools for Thermal-Aware Reliability Assessments of IC Designs

Project Staff
S. M. Alam, D. E. Troxel, and C.V. Thompson

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Integrated circuits are often designed using simple and conservative 'design rules' to ensure that the resulting circuits will meet reliability goals. This simplicity and conservatism leads to reduced performance for a given circuit and metallization technology. To address this problem, we had developed a TCAD tool, ERNI, which allows process-sensitive and layout-specific reliability estimates for fully laid out or partially laid out integrated circuits (Y. Chery, S. Hau-Riege) (see figure 1).

Circuit-level reliability analyses require reliability assessment of a large number of sometimes complexly connected interconnect trees. We have shown through modeling and experiments that the resistance saturation observed in straight via-to-via lines, which can lead to immunity from electromigration-induced failure, also occurs in more complex interconnect trees. We have also shown that trees will be 'immortal' if their effective current-density line-length product, $(jL)_{eff}$, is below a critical value. The jL product that defines immortality can be determined from experimental characterization or simulation of the reliability of straight via-to-via lines. Simple tests for tree immortality can be used in a hierarchical way to eliminate trees from further more computationally intensive reliability assessments. After filtering of immortal trees, the reliability of mortal trees must be assessed. This can be done through reliability simulations with individual trees, but this computationally intensive method should be reserved for the most problematic trees, those with the least reliability, and which are least convenient to 'fix' through layout modifications. We suggested computationally simple and conservative 'default' models for assessment of tree reliabilities based on the Korhonen analysis and have tested models and simulations through experiments on simple interconnect trees.

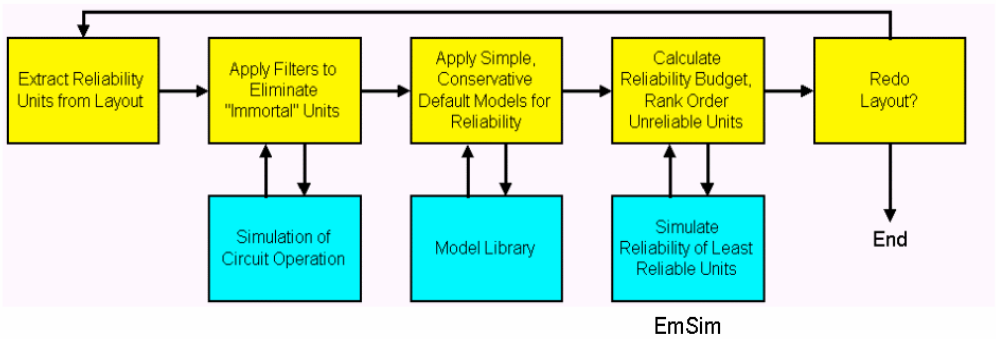

Figure 1: A flowchart for a full hierarchical circuit-level reliability assessment, the basis for the prototype tool ERNI.

Recent development in semiconductor processing technology has enabled the fabrication of a single integrated circuit with multiple device-interconnect layers or wafers stacked on each other. This approach is commonly referred to as the Three-Dimensional or 3D integration of ICs. Although there has been some research on the impact of 3D integration on chip size, interconnect delay, and overall system performance, the reliability issues in the 3D interconnect arrays are fairly unknown. We extended the reliability concepts in ERNI and developed a framework for reliability analysis in 3D circuits with a novel

Reliability Computer Aided Design (RCAD) tool, ERNI-3D. Both ERNI and ERNI-3D has recently been merged into a single RCAD tool, SysRel, capable of reliability analysis and comparison of 2D and 3D circuit layouts using aluminum (Al) as well as copper (Cu) interconnect technology.

As the 3D integration technology is not yet widespread, and no CAD tool supports IC layouts for such a technology, we first developed a comprehensive 3D circuit layout methodology. The circuit on each wafer or device interconnect layer can be laid out separately with inter-wafer via information embedded in the layout. The inter-wafer via information is generalized into three categories sufficient for defining all types of interconnection between wafers in a 3D stack (see figure 2). A strategy for layout-file management that incorporates the orientation of each wafer in the bonding process is also proposed. We have implemented the layout methodology in 3D-MAGIC, an extension of MAGIC originally developed at UC Berkeley and widely used in academia. The test circuits designed with 3D-MAGIC are a 3D 8-bit adder and an 8-bit encryption processor mapped into a 3D FPGA.

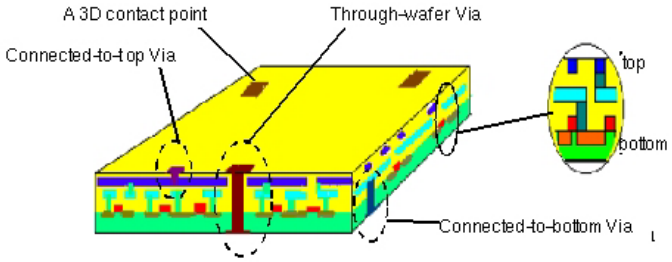

Figure 2: Different types of via/contact for 3D ICs.

In addition to circuit layout files in magic format, SysRel requires inputs for process parameters, immortality filter thresholds, and critical stress numbers for use in the reliability analysis flow. SysRel utilizes the hierarchical flow diagram for fundamental reliability unit (FRU) based electromigration analysis. When the vias form blocking boundaries for diffusion, an interconnect tree, defined as continuously connected conducting metal line in one layer of metallization ending at vias, is the FRU for electromigration reliability analysis. All FRUs are first extracted from a layout. For Cu interconnect technology, vias are classified as via-below or via-above. The FRUs are filtered out for immortality in two stages, first using a current density of j_{max} from the ITRS roadmap and then using j_{local} from circuit simulation. Via type based *jL* product thresholds are applied in the filtering stages for Cu technology. However, no such via classification is required for Al technology as a single *jL* product threshold is sufficient.

After the filtering stages, a technology (Al or Cu) specific analytical model is applied to the mortal FRUs to get expected lifetimes due to electromigration failure. Lifetimes are combined using a joint stochastic process for series system. Simulation results from SysRel with sample circuit layouts demonstrate the significance of our methodology in selectively identifying critical nets and their impacts on overall reliability.

As high temperature rise poses as a major challenge in stacked 3D ICs, we are currently working on circuit and system layout for thermal management and its impact on reliability. SysRel provides the required infrastructure for such a development. A novel feature being pursued in this activity is the capability to guide optimal placement of microfluidic *thermal connects* (see figure 3) at the layout-level. As a demonstration vehicle, we are focusing on structures of the type shown in the figure, in which device layers are bonded face-to-face (high density interconnects) and micromachined wafers are bonded back-to-back (low density through-wafer vias) to create channels for fluidic thermal connects. One of the key concepts is that while 3D stacked systems produce a heat generation problem, they also provide four more surfaces to use for heat extraction (or two pairs of surfaces for flow-through heat extraction).

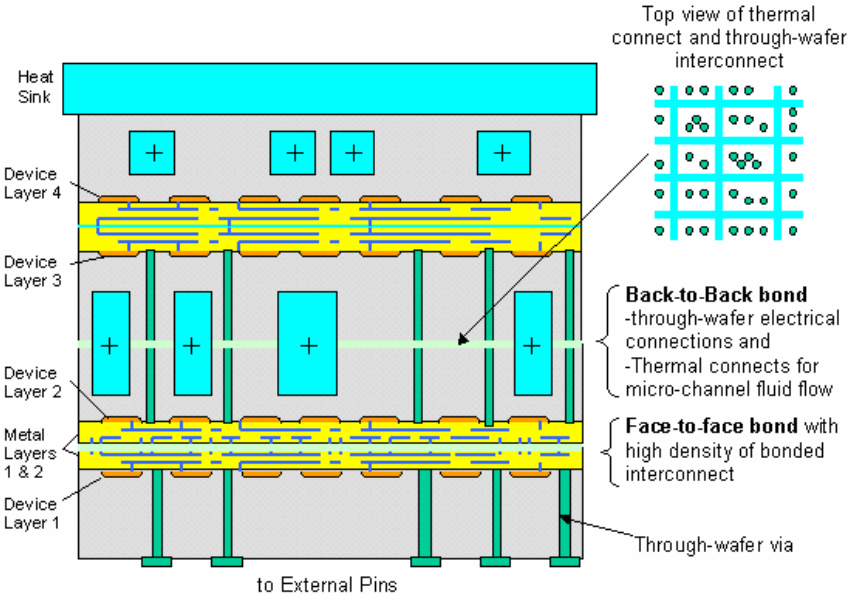

Figure 3: Thermal management in a 3D IC. Here the 3D IC is a 4-wafer bonded stack.

Publications

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