Quantum Nanostructures and Nanofabrication Group

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The Quantum Nanostructures and Nanofabrication Group focuses research on questions surrounding the application and fabrication of devices whose operation is based on the foundations of quantum mechanics. Because of the macroscopic extent of the superconductive wavefunction, superconductive devices are the most readily engineered examples of these types of devices. We therefore also focus on properties of superconductive materials. Finally, because quantum mechanical effects are primarily observable at microscopic length scale, a major component of our device research involves development and implementation of new methods of nanofabrication. Our interests include the architectural and system-related issues surrounding the application of quantum-mechanical devices to computation.

1. Progress in Developing Nanowire Photodetectors

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Single photon detection is useful for applications ranging from biomedical imaging and VLSI-electronics failure analysis to quantum and ultra-long-distance (perhaps even interplanetary) free-space optical communication. But the standard semiconducting single-photon detector, the avalanche photodiode, is limited to counting rates of a few MHz. We have developed a new fabrication process for a superconductive single-photon detector [1] with expected counting rate of ~ 10 GHz. The photodetector consists of a nanofabricated niobium nitride wire, and is expected to operate at a temperature of less than 10K. The enhanced performance relative to conventional detectors could be used to increase the bandwidth of both quantum communication and ultra-long-distance free-space optical communication.

The detector that we are currently developing consists of a narrow (ideally sub-100-nm-wide) superconducting wire in a boustrophedonic pattern that is current-biased to near its critical-current density. By biasing the detector with a current just below the critical current of a superconductor, the detector is prepared for photon detection. When an incident photon is absorbed by the narrow wire, the resulting hot spot constrains the passage of the current sufficiently to cause a transition out of the superconductive state, into the resistive state, which is then detected. The detector then relaxes to the superconducting state with a time scale of ~ 30 ps, resulting in a voltage pulse.[1]

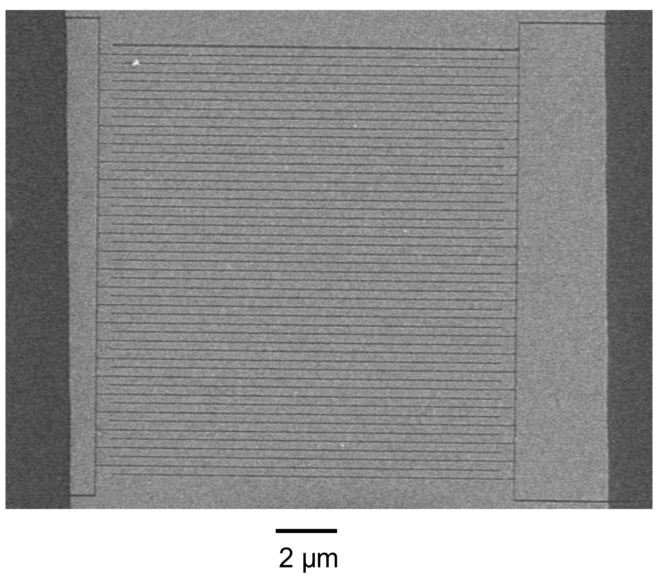

Figure 1.1: Photodetector fabricated in NbN. The wires shown are 225-nm wide, on a 300-nm pitch. The total detector area patterned is 15 μm × 15 μm.

The starting materials for this project were supplied by Prof. G. Gol'tsman at the Moscow State Pedagogical University, and consisted of between 3 and 10 nm of epitaxial niobium nitride grown on a sapphire substrate, and subsequently patterned into a 20 μm × 20 μm block, attached at opposite sides to tapered gold electrodes in a coplanar waveguide configuration [2]. We performed nanopatterning of this starting material.

Most nanoscale processing was performed in the RLE NanoStructures Laboratory, with the electron beam lithography done using the RLE Scanning-Electron-Beam Lithography facility. Our device dimensions were 225-nm wires on a 300-nm pitch (resulting in 75-nm-wide gaps between the turns of the meander). We used 80-nm thick PMMA resist as an etching mask. The final step in the processing was to transfer the patterned PMMA resist into the underlying NbN layer, for which we used reactive ion etching in CF_4 gas under 375 V bias and 15 mTorr. The photoresist was then removed using oxygen plasma ashing.

One of the most challenging aspects of the superconductive device processing is the problem of altering the superconductive properties of the material through either physical or chemical in-process damage. This damage is of particular concern when processing such thin films (in our case between 3 and 10 nm thick). To avoid damage, great care was taken to avoid any extraneous processing. During plasma processing the device leads were intentionally shorted through a low-resistance path to prevent device damage from plasma exposure. We also showed that errors in lithography could be successfully corrected using an oxygen plasma ash to remove the resist, without affecting the superconductivity of the device. The resulting photodetector exhibited characteristic superconductive behavior. We plan to investigate the device physics further in the coming year.

Our next action will be to integrate an optical cavity with the device, which will serve to permit multiple passes of light through the niobium nitride layer (thus enhancing the total efficiency of the detector) and to reduce the efficiency loss due to reflection. We also plan to explore alternative materials, such as MgB_2, for the detectors, as well as investigate methods of generating arrays of detectors for applications to imaging and adaptive optics.

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2. Progress in using Genetic Algorithms for Proximity-Effect Modeling of Electron-Beam Lithography

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Electron-beam lithography has become a standard for nanoscale patterning in research environments: it is the only broadly available tool that provides rapid and easy access to the sub-100-nm domain to university and industrial researchers alike. Despite its strengths, it suffers from several difficulties: (1) slow speeds (although in fact writing time is almost never an obstacle for small-scale manufacturing of high-value items); (2) the proximity effect, wherein electrons are scattered by the substrate and return to the surface to expose nearby regions of the resist. The proximity effect generally limits the uniformity of patterns with a spatially varying density.

This project aims at gaining a better understanding of the role of the proximity effect in writing of nanometer-scale single-photon detectors. We first are working to obtain experimental data concerning the pointspread function of the e-beam system exposing PMMA resist on sapphire [1]. We will then be able to use this data to model the actual exposure pattern given the nominal exposure pattern. We have executed a simulation using typical point-spread functions from the literature, and the results are shown in figure 2.1 below.

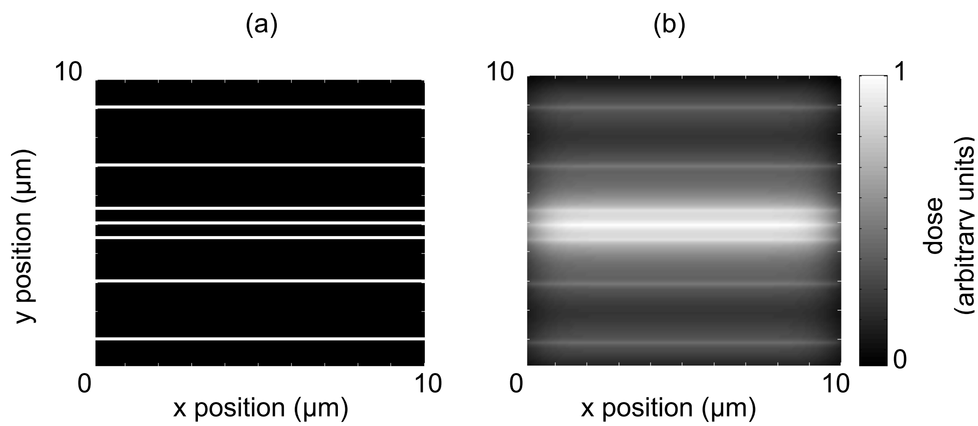

Figure 2.1: (a) dose matrix of a test pattern; (b) resulting dose received by resist using the data provided in [2] for 600nm-thick PMMA on silicon. Notice that densely spaced lines blur together due to the proximity effect

The more challenging problem is now to iterate the nominal pattern to be written and attempt to find a pattern that, when processed through our simulator, yields an exposure pattern closer to the ideal. Evolutionary algorithms are among the most efficient for identifying solutions in a high-dimensional search space, but have not been applied to this problem before.

At present, nanometer-scale photodetectors require a current bias as close as possible to the true switching current of the device in order to achieve maximal efficiency. But any narrowing in the device linewidth, even if only over a small region, limits the current that can flow. By implementing a genetic algorithm for proximity-effect elimination, we are working to optimize the shape of the photodetector and thus to improve its efficiency.

Acknowledgements

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3. Progress in using Genetic Algorithms for Evolvable Hardware Design

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Harnessing all of the intrinsic data-processing power of electronic devices is impossible through traditional circuit design. While complex physical processes involving electronic, thermal, and even quantum phenomena underlie the operation of the devices, standard circuit design methodology appropriately mandates a level of abstraction where most of these phenomena are safely ignored. This discipline permits rapid, effective design of circuits based on sound engineering principles. However this discipline also limits the data processing capabilities of the circuit. For example, thermal effects and cross-talk between circuit components are generally seen as limiting features, while, from a fundamental physics viewpoint they increase the phase space available to the system for data processing. A spectacular example of an instance where these previously neglected degrees of freedom proved enormously useful is quantum computing, where access to the vast phase space of the quantum wavefunction of the system results in a massive increase in the processing power. In this work, we investigate the possibility that similarly enhanced data processing capabilities exist in previously neglected classical degrees of freedom of a circuit [1].

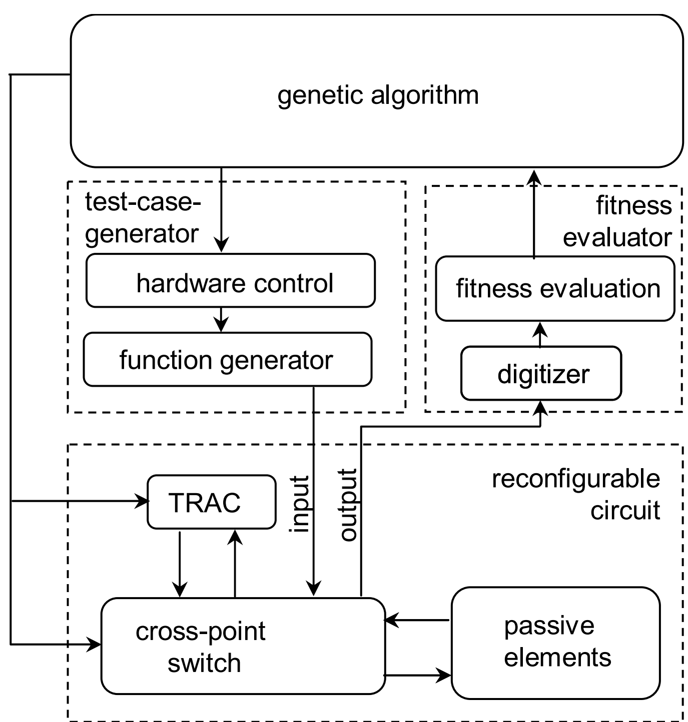

Fig 1. System representation for automated circuit design using an evolvable hardware approach.

Design that explicitly incorporates the full phase space of electronic devices into the standard design methodology is fraught with problems: noise, fabrication margins, and poorly understood interactions between the various physical degrees of freedom of the system, conspire to make a conventional approach difficult. Our approach instead uses reconfigurable hardware, in conjunction with a genetic algorithm (GA) to search for an optimal circuit configuration based on performance evaluated in hardware. In this approach, many of the limitations of traditional design are removed as the algorithm search is based on the input output performance and uses all degrees of freedom inherent in the system. Our specific goal is to test these ideas by generating an analog-to-digital converter using hardware evolution controlled by a GA.

Figure 1 shows the various design blocks being developed to achieve a working circuit evolved in hardware.

1.) The reconfigurable circuit itself: This consists of “Totally-Reconfigurable Analog Circuit” chips from Zetex, interfaced with passive circuit elements and each other through a cross-point switch array. Our use of a cross-point switch in this way is a departure from past work [2], and provides a way to scale the device to much larger levels of complexity.
2.) A test-case generator that creates a sample set of possible inputs for evaluation of the performance of the reconfigurable circuit.
3.) A fitness evaluator for establishing the performance of each test-case passed to the reconfigurable circuit.
4.) A genetic algorithm implemented in software, which takes in data from the fitness evaluator and calculates the next generation of circuits based on the results.

Our work to demonstrate an evolved circuit is motivated by two main applications: (1) processing applications where it could achieve sufficient raw-performance breakthroughs (such as increased circuit speed and reduced power consumption) to justify the inevitable added complexity of this approach; (2) fields like molecular electronics and quantum computing, where current fabrication tolerances are inadequate to satisfy the demands of the conventional design discipline. An example of a, optimization methods based on in-situ neural learning has already been considered by another group for programming nanodevices (where only poor control of circuit fabrication is usually achieved) [3]. Also of interest is quantum computation, where two challenges combine to make our approach relevant: (1) fabrication tolerances are insufficient at present to permit large scale application of the technology; and (2) very few appropriate algorithms now exist, making an automated-search approach to algorithm discovery an interesting alternative.

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