

3-D FPGA Design and CAD Flow

MTL / RLE Groups

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FPGA is an important programmable fabric for emerging systems. The performance and power dissipation of FPGAs is limited by interconnects (wires and switches). The 3-D FPGA is a next-generation FPGA with smaller wire-length, higher speed, and lower power consumption. We have developed a 3-D FPGA architecture, Figure 1, and simulated an implementation using a 0.18 μm three-layer 3-D integration technology.

The block diagram of our 3-D FPGA and with a simplified structure of the CLB (Configurable Logic Block) is shown in Figure 1. The basic unit of 3-D FPGA is a 3-D tile which is composed of a 3-D switch and a CLB. A 3-D mesh array of tiles constitutes a whole FPGA where wires of each 3-D switch are connected to that of nearest six switches. The CLB is composed of four sub-blocks with internal interconnection wires through multiplexers. Each sub-block is composed of a LUT (Look-Up Table), a flip-flop, and a multiplexer. In a 3-D tile, the 3-D switch is associated with a single CLB while the 3-D switch has interconnection wires connected to nearby 3-D switches. The 3-D switch interconnection and routing architecture are configurable with architecture parameters.

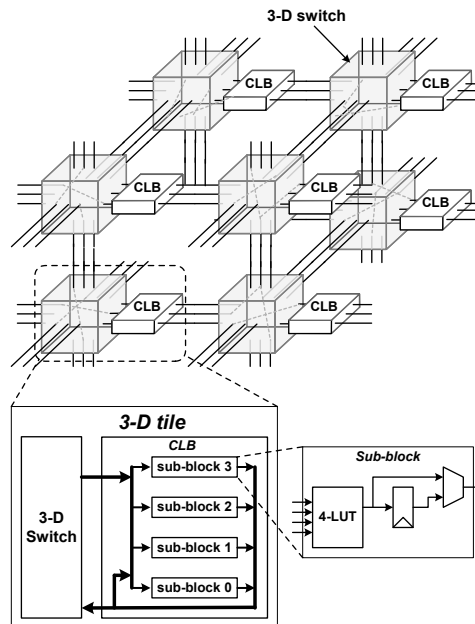


Figure 1. Block diagram of our 3-D FPGA architecture. The 3-D FPGA is composed of tiles where each tile is composed of 4 LUTs and 4 flip-flops.

We use a public domain tool to generate the netlist describing the interconnection among CLBs (packed netlist) from the circuit in BLIF (Berkeley Logic Interchange Format). The netlist has LUT configuration information as well as CLB packing information. The LUT configuration information is used for Verilog simulation to estimate the switching probability of the nets in the netlist. 3-D placement and routing considers speed, energy, and thermal characteristics for placing slices and routing nets in 3-D space. Our 3-D placement and routing is integrated with public domain tools to construct a complete 3-D FPGA CAD flow. Experimental results show 31% improvement in

the total wirelength, 46% improvement in the critical path delay, 44% improvement in the power consumption compared to 2-D FPGAs.

References:

[1] Young-Su Kwon, Payam Lajevardi, Anantha P. Chandrakasan, Frank Honorè, and Donald E. Troxel, "A 3-D FPGA Wire Resource Prediction Model Validated using a 3-D Placement and Routing Tool," in IEEE System-Level Interconnect Prediction, San Francisco, April 2005, pp. 65-71.

[2] A. Rahman, S. Das, A. P. Chandrakasan, and R. Reif, "Wiring requirement and three-dimensional integration technology for field programmable gate arrays," IEEE Transactions on VLSI Systems, Vol. 11, No. 1, pp. 44–54, 2003.