Integrated Systems

RLE Group
Integrated Systems Group

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Introduction

Integrated Systems Group is focused on several key design aspects of modern integrated systems. The group is focused on building cutting edge, energy-efficient integrated systems through vertical optimization encompassing communications and signal processing algorithms and architectures, and digital and mixed-signal circuits. The main research topics include modeling of noise and dynamics in circuits and systems, application of convex optimization to digital communications, analog and VLSI circuits.

Most integrated systems today are limited by tight power and/or throughput constraints. In this environment, the usual system hierarchy becomes inefficient and novel vertical system design approaches are needed to create overall most efficient integrated systems. We believe that this can be achieved by blurring of the strict hierarchy boundaries and modification of standard communication techniques and circuits to perform the operations in a most energy-efficient way.
Some of the example systems that we are interested in are high-speed electrical and optical interfaces, UWB transceivers and sensors, on-chip signaling, clock generation and distribution for system-on-a-chip.

1. Channel-and-Circuits-Aware, Energy-Efficient Coding for High-Speed Links

Sponsors
MARCO Interconnect Focus Center

Project Staff
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With state-of-the-art energy-efficiency of 40mW/Gb/s, links in a chip with 40Tb/s I/O throughput, for example, would dissipate 1.6kW of power, requiring 8000 high-speed I/O pins, and the on-chip area of 4000mm^2 for 4000 10Gb/s transceivers, in 0.13µm CMOS technology. The switch card would need to be at least 8 feet wide and have a 13-feet-wide connector with today's connector density limit of 50 differential pairs per inch. Clearly, we need to improve both the energy-efficiency of the link cells and per/pin data rate by at least an order of magnitude, to avoid excessive power dissipation and maintain a reasonable size of the system. This data rate scaling

is theoretically possible, since the information theoretic capacity of link backplane channels is between 80 and 110 Gb/s [1], as shown in Figs. 1 and 2.

By using multi-tone modulation in links [2] we not only increase the data rate of a link, but also decrease the energy cost of signaling per bit due to parallelism in frequency domain. Unfortunately, the gap of uncoded multi-tone modulation to capacity is still very big (around 14dB) due to very low BER target of 10^{-15} in these applications and the peak swing constraint of the on-chip driver circuits. The gap is even bigger in today's state-of-the-art baseband links, where residual interference from reflections and cross-talk limits the scaling of link data rates, requiring the use of costly reflection and cross-talk cancellers.

In this project we aim to extend the link system design to incorporate energy-efficient coding techniques. Using novel energy-efficient coding techniques for non-Gaussian noise and residual interference, we will both increase the achievable data rates and the energy-efficiency of links by drastically off-loading the low-BER target burden and hence decreasing the complexity of the equalization/modulation level. One theoretic footing of our work is based on our recent results in [1],[3], where a new framework was developed to systematically study energy efficient transmissions in a non-ideal environment, with time-varying link quality, peak-power constraint, processing energy overhead, and even modeling errors.

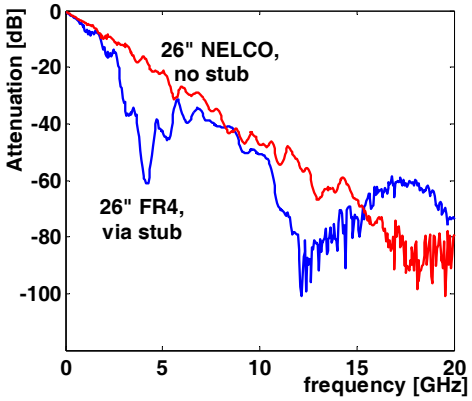

Figure 1: Legacy (FR4) and new, microwave-engineered (NELCO) backplane channels.

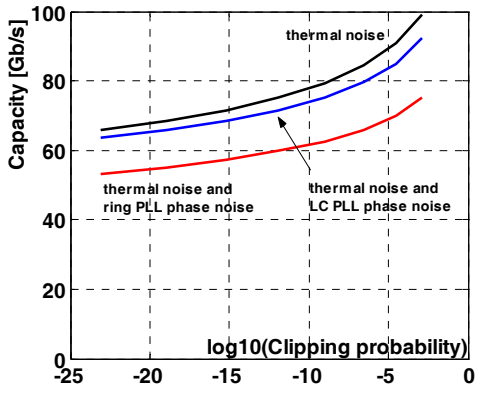

Figure 2: Legacy channel capacity with 50Ω termination thermal noise and phase noise from LC and ring VCO-based PLL.

References

[1] V. Stojanović, A. Amirkhany, M. Horowitz, "Optimal Linear Precoding with Theoretical and Practical Data Rates in High-Speed Serial-Link Backplane Communication," IEEE International Conference on Communications, pp. 2799-2806, June 2004.

[2] A. Amirkhany, V. Stojanović, M. Horowitz, "Multi-tone Signaling for High-speed Backplane Electrical Links," IEEE Global Communications Conference, pp. 1111-1117, December 2004.

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2. Convex Optimization of Integrated Communication Systems

Sponsors
Integrated Systems Group and Dawson research group

Project Staff
Ranko Sredojević, Tania Khanna, Professor Vladimir Stojanović and Professor Joel Dawson

Many integrated communication systems today are constrained by either throughput or power dissipation. Cases from high-speed I/O interfaces in processors and routers to low-power radios in cell phones and sensors force designers to tackle one of the two dual problems – optimizing the overall data rate with given power constraints or minimizing the power for given throughput. While much work has gone into both the circuit and communications sides of the problem, the hardest part seems to be communicating the requirements/costs and characteristics of circuits and components to the algorithm level and vice versa, so that the overall optimum can occur. Many design hours and iterations on the system architectures are needed before a system is designed and even then very little data exists on the scope of design space or the cost/performance space of the implemented components. What is the new optimal system if the specifications change slightly? To solve these problems, we intend to use the convex optimization as a framework to connect the circuit and system design abstractions.

We are developing a design-optimization framework in which an integrated communication system is constructed out of pre-characterized macros of analog, digital and mixed-signal circuits. Through the use of convex optimization, tradeoff functions and defined regions of operation are found for each macro. This information is then used at a higher–system design level to determine the right blend of algorithms and system architecture that implement a globally efficient communication system. This process is depicted in Fig. 1, on an example radio system. Convex optimization is critical to this effort, since it also provides the sensitivities of each objective function of the underlying circuit/block parameters, which builds intuition about the design and guides the designer in making intelligent topology changes. This challenging work is currently considered akin to black magic since the problem in general is combinatorial and NP-hard.

We intend to follow the work in [1]-[3] by putting their effort into a more general framework. We are currently building our own integrated circuit optimization flow. This will allow us not only to optimize a given circuit architecture, but also to explore different architectures, finding the ones that lend themselves nicely to convex optimization. We are currently working on a library of these adjustable or optimizable macros, such as mixers, VCOs, amplifiers, ADCs, DACs, and even their building elements. With this base and initial optimization results for each of the macros, we intend to engage in a system-level optimization on two example systems: a narrowband communication system (for example, a cell phone radio or a sensor) and a wideband communication system (an ultra-wideband radio or a multi-Gb/s high-speed chip-to-chip link [4],[5]).

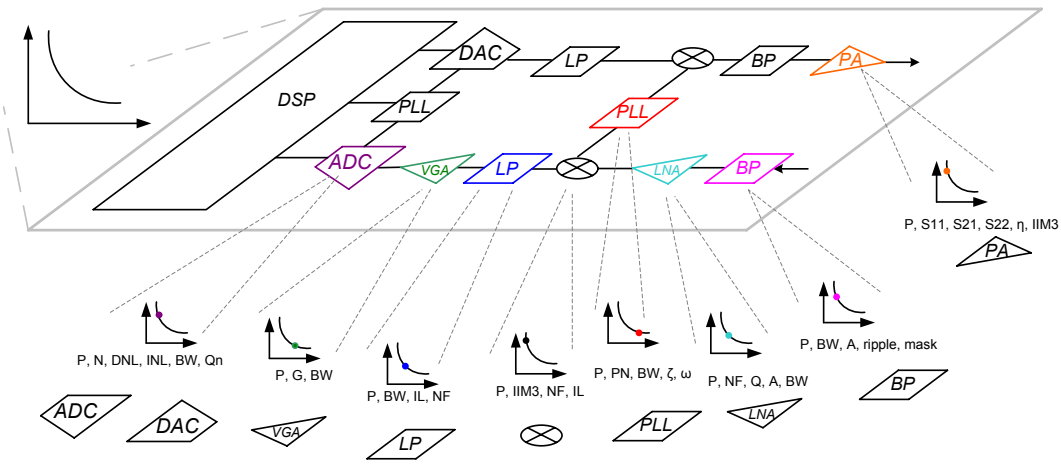

Figure 1: System-level partitioning: Underlying blocks optimized using convex optimization are described at the system level through the corresponding trade-off functions.

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[1] M. M. Hershenson, "Efficient Description of the Design Space of Analog Circuits," *Design Automation Conference*, pp. 970-973, 2003.

[2] M. M. Hershenson, "Design of Pipeline Analog-to-digital Converters via Geometric Programming," *ICCAD 2002*, pp. 317-324.

[3] D. M. Colleran, *et al*. "Optimization of Phase-locked Loop Circuits via Geometric Programming," *IEEE Custom Integrated Circuits Conference*, pp. 377-380, 2003.

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[5] V. Stojanović, A. Ho, B. Garlepp, F. Chen, J. Wei, E. Alon, C. Werner, J. Zerbe, M.A. Horowitz, "Adaptive Equalization and Data Recovery in a Dual-mode (PAM2/4) Serial Link Transceiver," *IEEE Symposium on VLSI Circuits*, June 2004, pp. 348-351.

3. Circuit and System Techniques for On-Chip Interconnects

Sponsors
Integrated Systems Group

Project Staff
Byungsub Kim and Professor Vladimir Stojanović

Signaling over global on-chip wires has been an increasingly difficult problem for the last several generations of VLSI technologies. As the technology scales, global wires scale poorly, causing a large increase in latency and forcing the system architects to focus on small, modular designs in which they can keep the cost of inter-module communication to scale approximately the same as the gate delay. Long interconnects are used only when necessary since in addition to the latency they require a significant amount of power due to repeater insertion needed to regenerate the signal along the interconnect. The goal of our project is to take a look at these interconnects as

micro-communication systems. We are developing signal conditioning and coding techniques that will take advantage of the interconnect channel properties and improve the data rate, latency, and power, while using very simple circuits. Our approach builds on the previous work on interconnects [1]-[3] by adding some of the techniques used in off-chip high-speed links [4].

From the perspective of communication channels, long interconnects exhibit different frequency-selective behavior depending on the geometry and density of the wires, as Fig. 1 shows. Depending on the geometry of the wires and the location of the current return paths, channels can exhibit dominantly dispersive (RC) behavior, or have slightly resonant behavior (RLC). Our initial results show that even in the lossy RC regime, we can obtain about a 2x improvement in the data rate over the current state-of-the art interconnect equalization technique [1], as Fig. 2 shows, with comparable if not potentially simpler circuits. We believe that the data rate and latency improvements are even higher in the RLC regime and plan to explore this next.

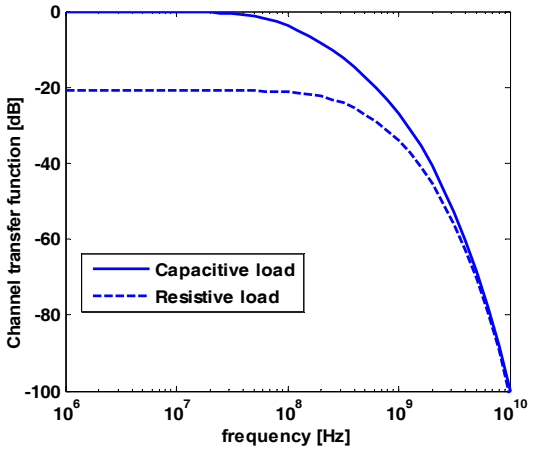

Figure 1: On-chip interconnect frequency response (10mm wire), RC regime, R_L=150Ω used in [1], and C_L=30fF used in this work.

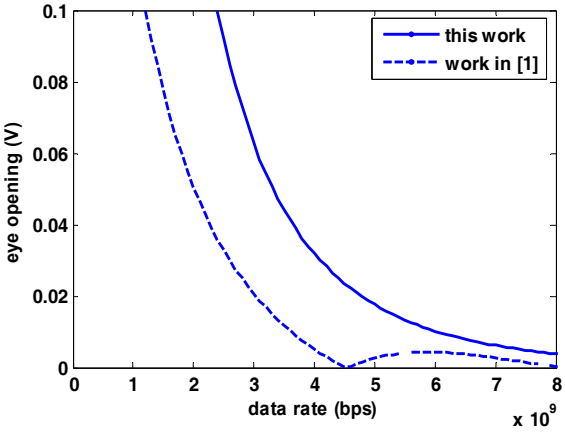

Figure 2: Eye-opening vs. data rate – comparison with [1].

References

[1] D. Schinkel, E. Mensink, E. Klumpernik, E. van Tuijl, B. Nauta, "A 3Gb/s Transceiver for RC-limited On-Chip Interconnects," in *Proceedings of IEEE International Solid State Circuits Conference*, February 2005.

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Publications

Meeting Papers, Presented

Vladimir Stojanović "High-Speed Links: Design Trends and Challenges", presented at the IEEE/LEOS Workshop on Interconnections within High Speed Digital Systems, May 8-11 2005.