Fine-Grain Power Control for Field Programmable Gate Arrays

Academic and Research Staff
F. Honoré, A. Chandrakasan, D. Troxel

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Implementation flexibility through hardware reconfiguration has become an important factor in the design of digital systems. Field Programmable Gate Arrays (FPGAs) are extending their application area from system prototyping to custom application implementation but they are much slower and less power-efficient than ASIC systems. We have developed a power- and performance-scalable multi-V_{DD} FPGA. The interconnect overhead for FPGAs is a large fraction of the power and delay, due to the use of programmable switch elements. Fine-grain voltage domains allow low-energy operation in non-critical areas of logic and routing segments.

We modified a public domain FPGA place-and-route tool to handle assignment of the voltage domains for non-critical paths. Thus, by selecting either a low or high voltage for each domain, this method achieves an average of 2X improvement in power for the same performance, as shown in Figure 1. The high V_{DD} is kept at 1.8V and the low V_{DD} can vary depending on the application. Low-overhead level converters provide voltage conversion between domains when necessary. With these fine-grain controls, the software is able to reduce dynamic power while maintaining performance. The area overhead for the power switches and level converters is less than 10%.

We have fabricated and tested a 3x3mm chip (Figure 2) using a semi-custom ASIC flow to validate the approach and have developed custom CAD tools to automate the implementation of some of these techniques. The test chip contains 64 tiles of logic. Testing confirmed functionality at a range of voltages from 1.8V down to 550 mV.

The chip was fabricated in 0.18-µm CMOS technology. We acknowledge National Semiconductor for providing IC fabrication services.

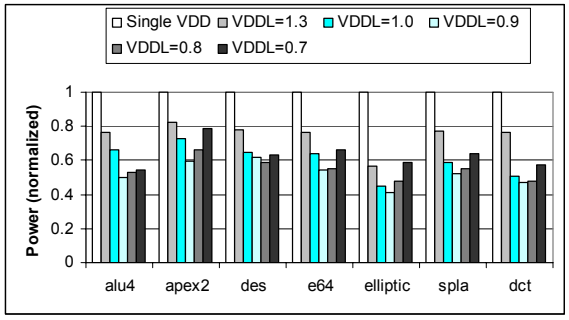

Figure 1: Benchmark results showing an average improvement of 52% at a V_{DDH} of 1.8V and V_{DDL} of 0.9V.

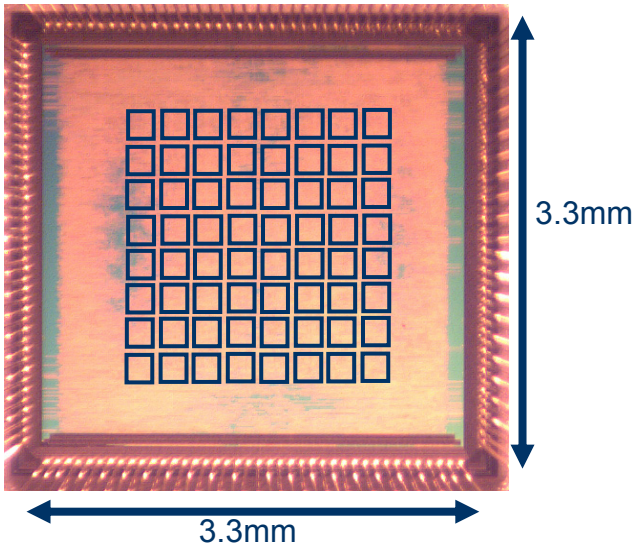

Figure 2: Die photo of fabricated test chip.

CAD for Tile-based 3-D Field Programmable Gate Arrays

Academic and Research Staff
Professor A.P. Chandrakasan, Professor D. E. Troxel

Graduate Students
Vikram Chandrasekhar

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This work analyzes the benefits of 3-D integration in terms of performance and power consumption in Field Programmable Gate Arrays (FPGAs). The VPR CAD tool [2] for 2-D FPGAs is modified to route circuits on a 3-D FPGA architecture. The placement is performed by a Simulated Annealing algorithm and the Pathfinder algorithm is used for routing the nets in the placed circuit. We are also exploring several architectural options such as optimal buffer insertion and the use of asymmetric switch matrix architectures for the 3-D FPGA. Also, the power consumption can be significantly reduced by using a lower supply voltage to achieve the same operating frequency as a 2-D FPGA. The graphs below show the relative critical path delays and estimated power consumption values for FPGAs with multiple layers.