Analog VLSI and Biological Systems

RLE Group
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Introduction

The group's research focuses on bioelectronics. We work on bio-inspired electronics, which takes inspiration from neurobiology to architect novel and efficient electronics, and on electronics for biomedical applications. Our research is interdisciplinary and lies at the interface between neurobiology and circuits. Theoretical models of neurobiological systems and experimental implementations of circuits with real-world impact are both very important to our research.

Neurobiology provides several examples of extremely power-efficient design. Power-efficient operation is very important for biomedical applications that need to run on a small implanted battery for several years. In both bio-inspired and biomedical electronics, analog computation is important for efficiency.

We concentrate on applying low power analog microelectronics to the design of bionic systems, mixed-signal computing systems and sensory systems. Traditionally, analog designers have relied on technology improvements or on a bag of circuit tricks to reduce power. Our emphasis is on achieving low power through fundamentally new architectures and topologies that are inspired by neurobiology, through feedback techniques that encode knowledge of the error or knowledge of the world into the structure of the circuit, through low-noise techniques that achieve precision without wasting power, through mixed-signal techniques, and by exploiting the power-efficient subthreshold region of MOS transistor operation.

1. Bionic Ear

Sponsors
David and Lucille Packard Foundation Fellowship, under contract number 2001-19533

Project Staff
Michael Baker, Timothy Lu, Christopher Salthouse, Ji-Jon Sit, Lorenzo Turicchia, Serhii Zhak,Professor Sarpeshkar

This project focuses on the design of ultra-low-power analog cochlear-implant processors, and on processors that take inspiration from the human ear to perform better in noisy environments. A recent success resulted in an analog bionic ear processor that cut power consumption by more than an order of magnitude over the best digital solutions. The power consumption of this processor is so low that it will enable 30 year operation on a 100mAh rechargeable battery. This project also explores the use of an analog silicon cochlea, which maps the biophysics of the inner ear to a chip, as the basis for a cochlear-implant processor. The silicon cochlea has the potential to revolutionize speech recognition and patient performance in the presence of background noise -- a critical limiting factor today – while doing hundreds of mega floating point operations per second on a modest mW of power. A novel ear-inspired companding algorithm that has shown excellent promise for improving recognition in noise is being mapped onto ultra-low-power electronic chips. These chips will be used in portable speech-recognition and cochlear-implant systems. Work on the silicon cochlea has shed insight into how the biological cochlea ingeniously converts a filtering problem that scales quadratically into an easier problem that scales linearly. A new project in the lab is researching how to build an “RF cochlea”, an ultra-wide-band spectrum analyzer that mimics the traveling-wave architecture of the cochlea, but at RF frequencies.

2. Time-Based Hybrid Computing

Sponsors
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Project Staff
Micah O’Halloran, Heemin Yang, Professor Sarpeshkar

This project attempts to combine the best of analog and digital computation to perform computations more efficiently than either individual paradigm can accomplish alone. The goal is to combine the analog advantages of low power and good technology exploitation with the digital advantages of divide-and-conquer processing, signal restoration, and programmability. This work is based on the dual nature of signal representation of the brain’s neurons, which appear to have features of both analog pulse-time and digital pulse-count signal processing. Some fruits of this research include an ultra-low-power time-based analog-to-digital converter that improves the conversion efficiency of conventional time-based techniques from exponential to linear and a record-setting analog memory element. Hybrid State Machines built with this approach are being explored for designing novel control architectures, for ultra-low-power speech and sequence recognition, and for designing programmable vision chips.

3. Analog VLSI Vision Systems

Sponsor
Catalyst Foundation Fellowship

Project Staff
Maziar Tavakoli-Dastjerdi, Micah O’Halloran, Professor Sarpeshkar

This project uses low-power bio-inspired photoreceptors as front ends for analog VLSI motion sensors and in pulse oximetry for vital-sign monitoring of medical patients. Analog motion sensors are inspired by correlation circuits in houseflies and are important in robotic, security camera, and web-camera applications.

Publications

Journal Articles, Published

H. Yang and R. Sarpeshkar, "A Time-Based Energy-Efficient Analog-to-Digital Converter," *IEEE Journal of Solid-State Circuits* 40(8): 1590-1601 (2005).

T. Lu, S. Zhak, P. Dallos, and R. Sarpeshkar, "Fast Cochlear Amplification with Slow Outer Hair Cells," *Hearing Research* 214(1-2): 45-67 (2006).

R. Sarpeshkar, "Brain Power: Borrowing from Biology Makes for Low-Power Computing," *IEEE Spectrum* 43(5): 24-29 (2006).

Journal Articles, Accepted for Publication

C. Salthouse and R. Sarpeshkar, "Jump Resonance: A Feedback Viewpoint and Adaptive Circuit Solution for Low-Power Active Analog Filters," *IEEE Transactions on Circuits and Systems I*, forthcoming.

M. Baker and R. Sarpeshkar, "Low-Power Single Loop and Dual-Loop AGCs for Bionic Ears," *IEEE Journal of Solid-State Circuits*, forthcoming.

J. J. Sit, A. M. Simonson, A. J. Oxenham, M. A. Faltys, and R. Sarpeshkar, "A low-power asynchronous interleaved sampling algorithm for cochlear implants that encodes envelope and phase information," *IEEE Transactions on Biomedical Engineering*, forthcoming.

Journal Articles, Submitted for Publication

A. J. Oxenham, A. M. Simonson, L. Turicchia, and R. Sarpeshkar, "Evaluation of companding-based spectral enhancement using simulated cochlear-implant processing," submitted to *JASA*.

B. Raj, L. Turicchia, B. Schmidt-Nielsen, and R. Sarpeshkar, "An FFT-based Companding Front end for Noise-Robust Automatic Speech Recognition," submitted to *IEEE Trans. Speech Audio Proc.*

L. Turicchia, K. Kasturi, P. Loizou, and R. Sarpeshkar, "Evaluation of the companding algorithm for noise reduction in cochlear implants," submitted to *JASA*.

H. Yang and R. Sarpeshkar, "A Bio-inspired Ultra-Energy-Efficient Analog-to-Digital Converter for Biomedical Applications," submitted to *IEEE Transactions on Circuits and Systems I*.

M. Tavakoli-Dastjerdi and R. Sarpeshkar, "An Ultra-Low-Power Pulse Oximeter Implemented with Logarithmic Photoreceptors," submitted to *IEEE Transactions on Biomedical Engineering*.

Meeting Papers, Presented

A. M. Simonson, A. J. Oxenham, L. Turicchia, and R. Sarpeshkar, "Evaluation of Companding-Based Spectral Enhancement Using Simulated Cochlear Implant Processing," paper presented at the Meeting of the American Auditory Society, Scottsdale, Arizona, March 5-7, 2006.

Meeting Papers, Published

T. Lu, S. Zhak, P. Dallos, and R. Sarpeshkar, "A Micromechanical Model for Fast Cochlear Amplification with Slow Outer Hair Cells," *Proceedings of the International Symposium on Auditory Mechanisms: Processes and Models*, Portland, Oregon, July 23-28, 2005.

P. Loizou, K. Kasturi, L. Turicchia, R. Sarpeshkar, M. Dorman, and T. Spahr, "Evaluation of the Companding and Other Strategies for Noise Reduction in Cochlear Implants," *Proceedings of the Conference on Implantable Auditory Prostheses*, Pacific Grove, California, July 30-August 4, 2005.

M. O'Halloran and R. Sarpeshkar, "An Analog Storage Cell with 5 electron/sec Leakage," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS 2006)*, Kos, Greece, May 21-24, 2006.

S. Mandal, S. Zhak, and R. Sarpeshkar, "Circuits for an RF Cochlea," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS 2006)*, Kos, Greece, May 21-24, 2006.

B. Kim, S. Mandal, and R. Sarpeshkar, "Power-adaptive Operational Amplifier with Positive-Feedback Self Biasing," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS 2006)*, Kos, Greece, May 21-24, 2006.

S. Mandal, S. K. Arfin, and R. Sarpeshkar, "Fast Startup CMOS Current References," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS 2006)*, Kos, Greece, May 21-24, 2006.

Theses

A. Selbst, *Clock Division as a Power Saving Strategy in a System Constrained by High Transmission Frequency and Low Data Rate*, MEng thesis, Department of Electrical Engineering and Computer Science, 2005.

M. Tavakoli-Dastjerdi, *An Analog VLSI Front End for Pulse Oximetry*, Ph.D. thesis, Department of Electrical Engineering and Computer Science, 2005.

H. Yang, *An Energy-Efficient Time-Based Analog-to-Digital Converter*, Ph.D. thesis, Department of Electrical Engineering and Computer Science, 2006.