Integrated Systems

Academic and Research Staff
Professor Vladimir Stojanović

Collaborators
Prof. Lizhong Zheng, Prof. Joel Dawson

Graduate Students
Nataša Blitvić, Fred Chen, Byungsub Kim, Maxine Lee, Sanquan Song, Ranko Sredojević,

Administrative Staff
Janice Balzer

Introduction

Integrated Systems Group is focused on several key design aspects of modern integrated systems. The group is focused on building cutting edge, energy-efficient integrated systems through vertical optimization encompassing communications and signal processing algorithms and architectures, and digital and mixed-signal circuits. The main research topics include circuit and system design for on-chip and off-chip interconnects, circuit optimization and design methodology, modeling of noise and dynamics in circuits and systems, application of convex optimization to digital communications, analog and VLSI circuits.

Most integrated systems today are limited by tight power and/or throughput constraints. In this environment, the usual system hierarchy becomes inefficient and novel vertical system design approaches are needed to create overall most efficient integrated systems. We believe that this can be achieved by blurring of the strict hierarchy boundaries and modification of standard communication techniques and circuits to perform the operations in a most energy-efficient way.
Some of the example systems that we are interested in are high-speed electrical and optical interfaces, silicon-photonics, metrology for carbon-nanotubes, on-chip signaling and networks, joint circuit and system optimization of a high-speed link, clock generation and distribution for system-on-a-chip.

1. Channel-and-Circuits-Aware, Energy-Efficient Coding for High-Speed Links

Sponsors
FCRP Interconnect Focus Center

Project Staff
Nataša Blitvić, Professor Lizhong Zheng and Professor Vladimir Stojanović

In order to achieve high throughput while satisfying energy and density constraints, both the data rates and the energy efficiency of high-speed chip-to-chip interconnects need to increase. This project aims to extend the link system design to incorporate energy-efficient channel coding techniques. Since high-speed links are intersymbol interference (ISI)-dominated environments, the effect of constraining the transmit alphabet on the decision distance needs to be taken into account. To enable the systematic characterization of different codes, we have therefore developed a simple divide-and-conquer algorithm [1] which quickly and accurately computes the effect of a given systematic linear block code on the marginal probability distribution of the received signal. The resulting probability distributions are accurate at all points, including in the tails. Due to complexity constraints this method is of most use for high-rate codes, but is valid for both arbitrarily long codewords and arbitrarily long channel responses.

Integrating the probability distributions computed through the previously described technique yields marginal cross-over probabilities for different bit locations within a codeword. Comparing these to the cross-over probability of an uncoded system indicates the extent to which the coding constraints affect the performance of a system with ISI. Figures 1 and 2 illustrate this effect for two different link channels. Although the present focus is on simple codes with distance-enhancing properties, the current framework also allows for the characterization of classical error-detecting codes over interference-dominated channels. For links with relatively well-compensated interference and low noise correlation, the channel can be approximated as binary-symmetric. The individual crossover probabilities are therefore sufficient to compute the error probabilities *after* error correction. This property was verified in [1] for some typical link channels and down to BERs achievable by Monte Carlo simulation.

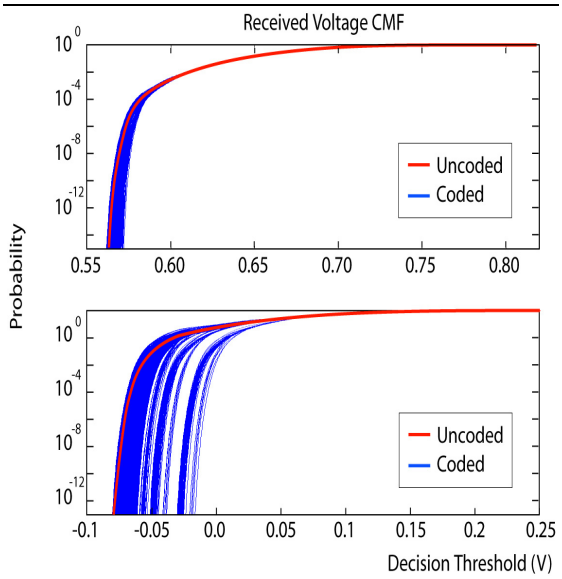

Figure 1: Voltage distributions for the set of all (10,8) linear block codes. Shown are the cumulative mass functions (CMF) for two different channels: Peters B3 operating at 5 Gbps [top] and Peters B32 operating at 10 Gbps [bottom]. The plots also show the voltage CMF computed under the assumption that the data is uncoded.

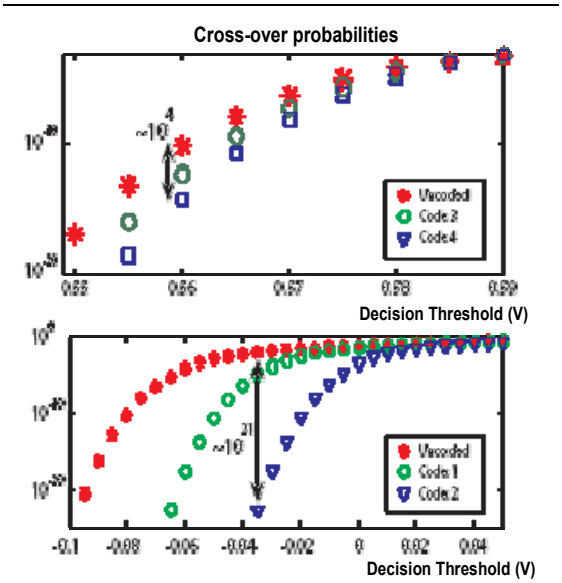

Figure 2: Bit crossover probabilities for the uncoded case and two different (10,8) linear block codes on a B3 channel [top] and B32 channel [bottom]. Code 2 was chosen to yield the maximum deviation from the uncoded CMF, while Code 1 was chosen roughly in between the two extremes. The results are computed under the common assumption that the link noise is additive, white and Gaussian with $\sigma \approx 3$mV.

References:

[1] N. Blitvic and V. Stojanovic, "A new statistical simulator for block-coded channels with long residual interference," *IEEE International Conference on Communications*, June 2007.

2. Optimization-driven System and Circuit Level Design of High Speed Links

Sponsors:
MIT Center for Integrated Circuits and Systems / FCRP Focus Center for Circuit & System Solutions (C2S2)

Project Staff
Ranko Sredojević, Professor Vladimir Stojanović

Currently, we aim to bridge the gap between analog/mixed-signal circuit and system design, by providing a framework for fast design space exploration at the system-to-circuit level, based on the bottom-up information from the underlying circuits and process technology, circuit and system designers.

This gap is particularly severe in high-speed link I/O circuits, which are rapidly growing into mini-communication systems due to the bandwidth limitations of packages and board traces [1]. Finding good methods to compensate intersymbol interference, minimize timing noise, while running circuits at lowest possible power and maximum possible data rate is a difficult balancing act that requires extremely tight connection between circuit and system level.

We try to provide a missing link between the system and circuit levels by formulating the system-to-circuit high-speed link description. This framework intimately connects circuit level parameters with block and system-level link specification, providing a direct vertical link from transistor sizes and parasitic to top level link metrics - data rate, power and bit error rate. We want this framework to provide answers to questions that link designers often ask: Which equalization method should be used (transmit pre-emphasis, linear analog receiver equalizer, decision-feedback equalizer)? What is the power/data-rate trade-off?

In Fig.1 we show the trade-off for a high-speed link with one-tap of transmit pre-emphasis and with receiver pre-amplifier equalization. When coupled with transmit pre-emphasis, receiver amplification improves the power-data rate trade-off since receiver pre-amplifier can drive larger on-chip impedance.

Next, in Fig.2 we show transmitter tap coefficients *w* for data rates in Fig.1. At lower data rates, where channel attenuation is not too strong, receive equalizer is very efficient taking on most of the equalization and amplification role. At higher loss conditions, the residual ISI in the channel saturates the input range of the receiver equalizer and transmit pre-emphasis has to increase to narrow down the dynamic range of the signal at the input to the receiver.

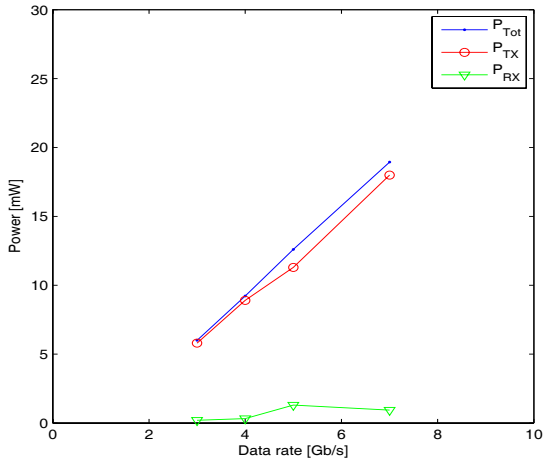

Figure 1: Power vs. data rate trade-off

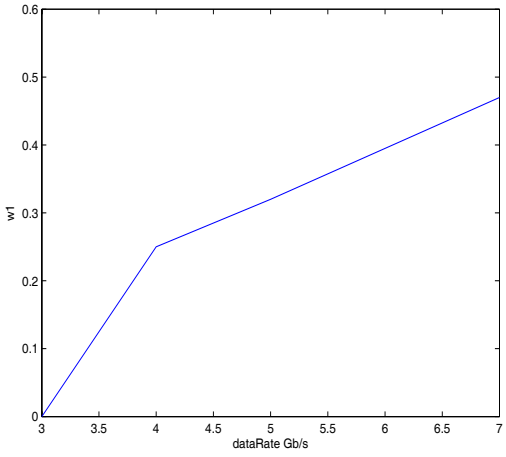

Figure 2: Transmitter side tap coefficient

References:

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3. Efficiency of High Speed On-Chip Interconnects: Trade-Off and Optimization

Design and Optimization of Equalized Interconnect for Energy-Efficient On-Chip Networks

Sponsors:
NEC fund and IBM faculty award

Project Staff
Byungsub Kim, Professor Vladimir Stojanović

In recent high performance processor design, cross-layer optimization of on-chip network and overall chip architecture has been shown to significantly improve the performance-power efficiency [1]. Though equalized on-chip interconnects [2,3] have been proposed to improve the network efficiency over traditional repeated interconnects, the optimization of equalized interconnect has been a difficult problem due to its design complexity.

This work presents a modeling and tool framework for fast design space exploration of equalized on-chip interconnects by exporting abstracted low level design parameters to a link model [4]. Using this tool technique, we can explore how the transistor and wire parameters affect link performance, equalization coefficients and architecture-friendly metrics like delay, power, and area throughput density. With this approach, we are able to find the best link design for target throughput power and area constraints, thus enabling the architectural optimization of energy-efficient on-chip networks.

Figure 1 shows the hierarchical simulation framework. The lower level models are abstracted into the higher level models. For example, RLGC matrices of the wire's transmission line are used to derive the through and crosstalk closed form transfer functions of the channel. At the top level, the behavioral model simulator uses the transfer functions to compute the link metrics and provides interconnect metrics for a low common mode (LCM) type equalized interconnect [5].
Figure 2 shows optimization results comparing interconnect metrics between the LCM and the repeated interconnects. Our simulation shows that the equalized LCM interconnect is much more power efficient than the repeated interconnect for given target throughput density.

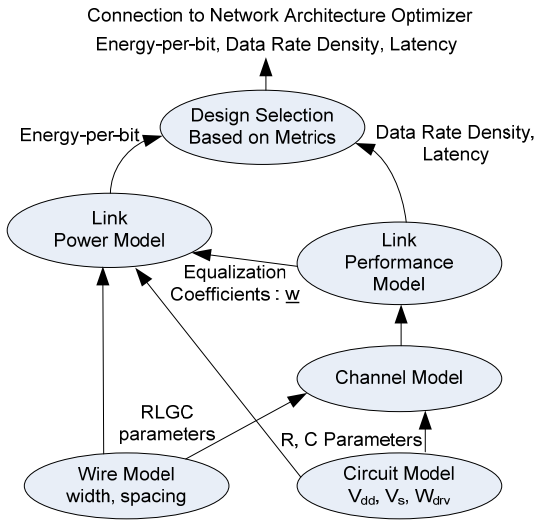

Figure 1: Hierarchical simulation framework

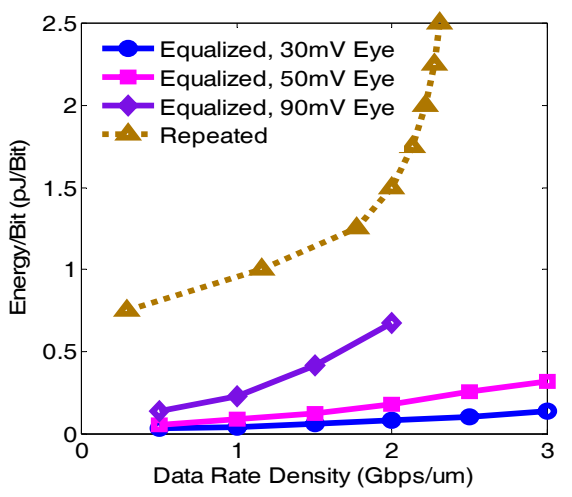

Figure 2: Interconnects throughput density and power density trade-off

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[4] B. Kim and V. Stojanović "Equalized Interconnects for On-Chip Networks: Modeling and Optimization Framework," *to appear at IEEE/ACM International Conference on Computer Aided Design*, Nov. 2007.

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[1] J. Ren, H. Lee, O.h. Dan, B. Leibowitz, V. Stojanović, J. Zerbe and N. Nguyen "Performance Analysis of Edge-based DFE; Accurate System Voltage and Timing Margin Simulation in CDR Based High Speed Designs," *Electrical Performance of Electronic Packaging; Electrical Performance of Electronic Packaging*, pp. 265; 171-268; 174, 2006.

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