CAD for Tile-based 3-D Field Programmable Gate Arrays

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A CAD tool has been developed to specify 3-dimensional FPGA architectures and map RTL descriptions of circuits to these 3-D FPGAs. The CAD tool was created from the widely used VersatilePlace and Route (VPR) CAD tool for 2-D FPGAs. The tool performs timing-driven placement of logic blocks in the 3-dimensional grid of the FPGA using a two-stage Simulated Annealing (SA) process. The SA algorithm in the original VPR tool has been modified to focus more directly on minimizing the critical path delay of the circuit and hence maximizing the performance of the mapped circuit. After placing the logic blocks, the tool generates a Routing-Resource graph from the 3-D FPGA architecture for the VPR router. This allows the efficient Pathfinder-based VPR router to be used without any modification for the 3-D architecture.

The work also proposes a dual-interconnect architecture for 3-D FPGA which has parasitic capacitance comparable to 2-D FPGAs. The nets routed in a 3-D FPGA are divided into intra-layer nets and inter-layer nets, which are routed on separate interconnect systems. We use a technique called I/O pipelining which pipelines the primary inputs and outputs of the FPGA through unused registers. This 3-D architecture and I/O pipelining technique have not been found in any of the works proposed so far, in the area of 3-D FPGA design. It is shown that the Dual-Interconnect I/O pipelined 3-D FPGA on an average achieves 43% delay improvement and in the best case, up to 54% for the MCNC'91 benchmark circuits.