

## Integrated Systems

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### Introduction

Integrated Systems Group is focused on several key design aspects of modern integrated systems. The group is focused on building cutting edge, energy-efficient integrated systems through vertical optimization encompassing communications and signal processing algorithms and architectures, and digital and mixed-signal circuits. The main research topics include circuit and system design for on-chip and off-chip interconnects, circuit optimization and design methodology, modeling of noise and dynamics in circuits and systems, application of convex optimization to digital communications, analog and VLSI circuits.

Most integrated systems today are limited by tight power and/or throughput constraints. In this environment, the usual system hierarchy becomes inefficient and novel vertical system design approaches are needed to create overall most efficient integrated systems. We believe that this can be achieved by blurring of the strict hierarchy boundaries and modification of standard communication techniques and circuits to perform the operations in a most energy-efficient way. Some of the example systems that we are interested in are high-speed electrical and optical interfaces, silicon-photonics, metrology for carbon-nanotubes, on-chip signaling and networks, joint circuit and system optimization of a high-speed link, clock generation and distribution for system-on-a-chip.

## 1. On-chip, High-frequency Characterization of Carbon Nanotubes

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FCRP Interconnect Focus Center

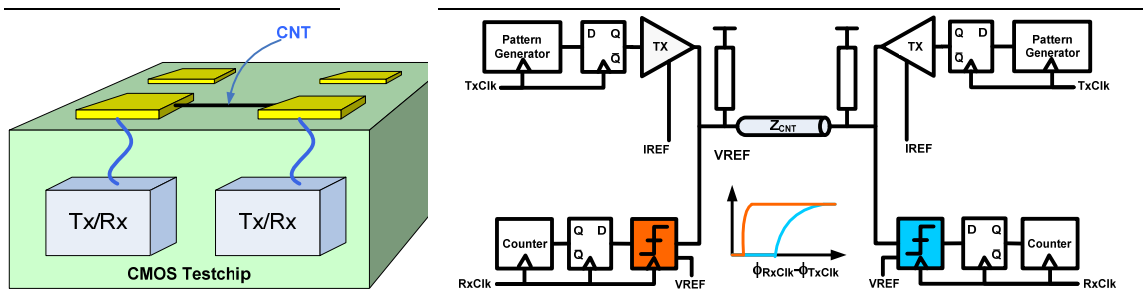
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Measuring the high-frequency characteristics of nanoscale devices such as CNTs and nanowires is a critical step in determining their viability for semiconductor applications [1]. Previous efforts to measure high-frequency characteristics of CNTs have been limited by a handful of common problems. First, the traditional approach of using a network analyzer (VNA) to capture the frequency response is limited by the poor power transfer between the high impedance ( $> 10 \text{ k}\Omega$ ) of the device and the  $50 \text{ }\Omega$  test equipment termination. This impedance mismatch offsets the selective bandwidth of the VNA used to reduce the noise floor, resulting in a large variance of measured data due to signals being at or near the noise floor. Second, measurement parasitics from test probes and pads often dominate the reactance of the CNTs being measured, limiting both the accuracy of the results and the bandwidth of the measurement. Third, given the dimensions of CNTs, test setups are difficult to reproduce, limiting the range of lengths and

number of CNTs that can be measured.

To address these issues, we have developed an on-chip test platform consisting of an array of 256 transceivers. Figure 1 shows a conceptual drawing of the CNT to CMOS test chip interface. Under each pad in the array is a transceiver that is independent of all others, allowing for measurement between any two pads in the array. Figure 2 shows the top level block diagram of two transceivers linked by a CNT “channel.” Similar to [2] but with mostly on-chip components, the step response of the channel is captured by changing the threshold voltage of the sampler (VREF) and the relative phase of the receiver clock (RxClk) with respect to the transmit clock (TxClk). Each transceiver has an adjustable termination and employs a capacitance compensation technique to allow full-sized bond pads for device characterization at the chip interface while maintaining input drive bandwidths up to 1GHz for a 4 kΩ termination. A 20-bit counter accumulates samples at each point, to average out timing noise due to jitter and any dynamic voltage offsets in the sampler.



**Figure 1:** Conceptual drawing of the CNT to CMOS test chip interface.

**Figure 2:** Block diagram of 2 transceivers linked by a CNT and conceptual waveforms captured by shifting VREF and RxClk.

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## 2. Iterative Robust Optimization of Analog Circuits

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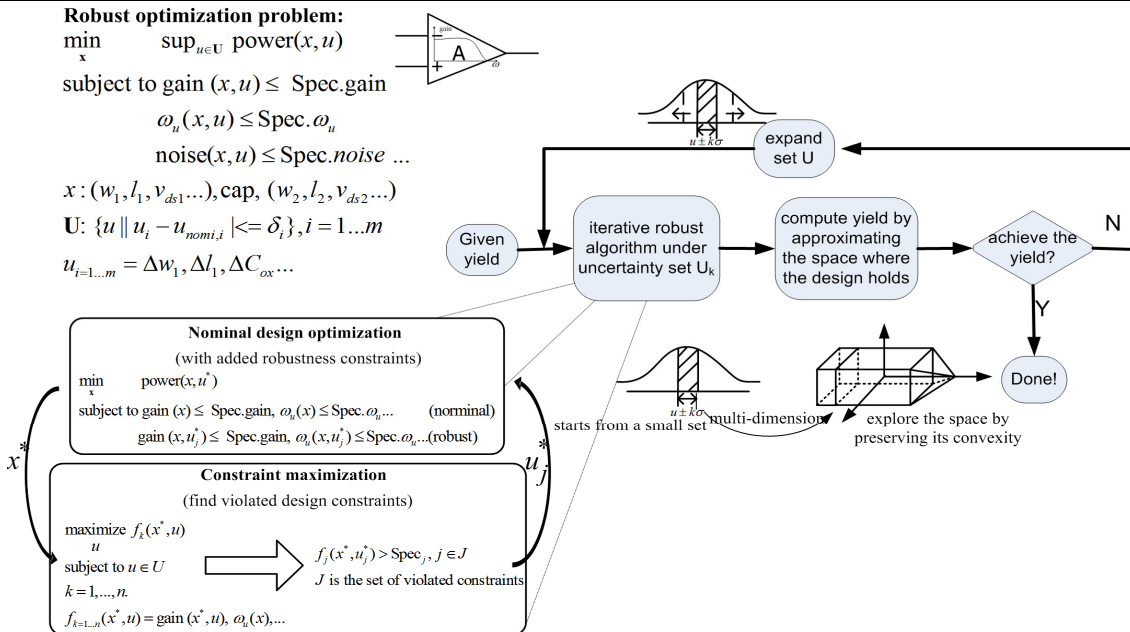
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As IC technologies scale down to the deep submicron region, process variation is becoming an increasingly severe issue for circuit designers. Designs are verified over process corners to improve the robustness of circuits and increase the manufacturing yield. However, it requires long design periods and often leads to overdesign. We are trying to develop new numerical algorithms fitted into an equation-based circuit optimization methodology, which incorporates the process variations, as well as provides yield estimation.

Inspired by the algorithm used in a robust taper design [0], we have developed and implemented the iterative robust optimization algorithm as shown in the left blocks in Figure 1. Rather than formulate the problem into a stochastic optimization problem as done in some previous work [0], we propose a more practical way. The optimization problem runs iteratively, with added robust constraints in each iteration. Thus, the optimization problem size grows, resulting in a more and more robust system. Relying on a fast optimization solver, the growing problem can still be solved efficiently. As an example, a two stage opamp could be designed with robustness within minutes. The left flow in Figure 1 shows an outer loop around the iterative algorithm to generate a yield-aware design. The algorithm starts from a design with small process variation range and the yield gets estimated. The variation ranges keep growing until the yield gets to the desired value. This approach could enable rapid generation of trade-off surfaces for desired circuit blocks, parameterized by yield.



**Figure 1.** Robust optimization problem formulation and the iterative robust optimization algorithm as shown on the left. Block diagrams on the right show the yield estimation flow.

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**Digital Equalization of the Nonlinear Photonic Modulator Diode**

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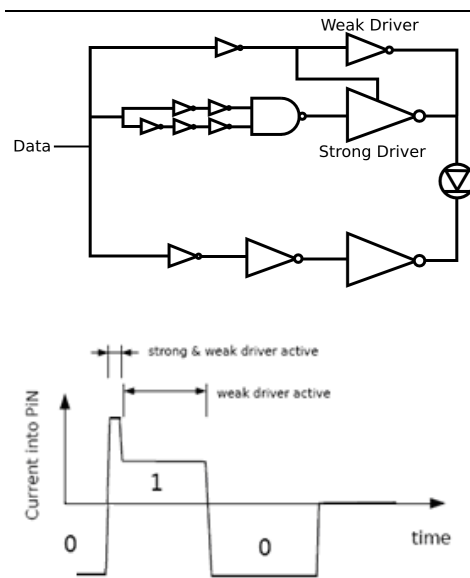
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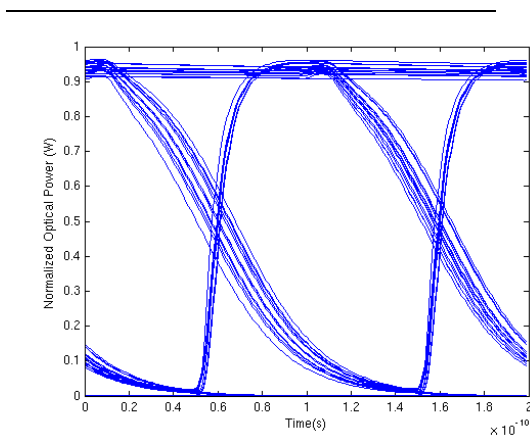
Electro-optical modulators are fundamental building blocks in on-chip photonic systems. On-chip optical waveguides can be created from thin unsilicided polysilicon tracks in a bulk CMOS process. The index of refraction of the poly waveguide depends on the charge concentration in the waveguide. Varying this charge concentration changes the phase of the light through the waveguide. In order to inject large amounts of charge into the waveguide more effectively, a P-I-N diode structure is created with the waveguide acting as the intrinsic region (I region) and N- and P-type doping added on either side of the waveguide.

We modified an existing SPICE model [1-2] of a P-I-N diode to model the photonic modulator. Figure 1 shows a digital circuit that controls the amount of charge entering the I region. This circuit uses a push-pull topology with pre-emphasis. The pre-emphasis controls the amount of charge that must enter and leave the I region for each bit, lowers the energy per bit, and prevents the ring's optical passband from shifting into the next optical channel. At the beginning of a zero-to-one transition, both the strong driver and the weak driver are active, maximizing the current into the I region. After a short time, the strong driver deactivates, lowering the current into the diode. The unbalanced weak driver has a strong NMOS and a weak PMOS. The strong NMOS ensures that the device quickly discharges through the I region for a one-to-zero transition. Figure 2 shows the simulated eye diagram for 10Gb/s.

Two flavors of this ring modulator were taped out with a 65-nm TI process. One modulator has a larger weak driver to account for varying carrier lifetimes in the diode. The energy efficiency is predicted to be approximately 50 fJ/bit.



**Figure 1** Abstract modulator diagram and its corresponding pre-emphasized current profile for a 010 input bit pattern. The weak driver has a very strong NMOS and a weak PMOS.



**Figure 2** Simulated eye diagram for 10Gb/s, assuming a 1-ns carrier lifetime.

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