

## Quantum Nanostructures and Nanofabrication

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The Quantum Nanostructures and Nanofabrication Group investigates the application and fabrication of devices using the foundations of quantum mechanics. We focus on: (1) superconductive devices and materials applied single-photon detection and quantum computing; (2) nanofabrication methods; and (3) applications of nanofabrication to energy systems. Superconductive devices are among the most readily engineered examples of devices exhibiting quantum-mechanical effects. We therefore work with superconductive materials, including efforts in materials, processing, and analysis. Also, because quantum-mechanical effects are primarily observable at microscopic length scale, we develop and implement novel methods of nanofabrication. We take a multi-disciplinary approach to these topics, borrowing techniques from physics, electrical-engineering, computer science, chemistry, and materials science.

## 1. Trapping ions with a superconducting ion trap

### Sponsors:

NSF Center for Ultracold Atoms, the Japan Science and Technology Agency and MIT

### Project Staff:

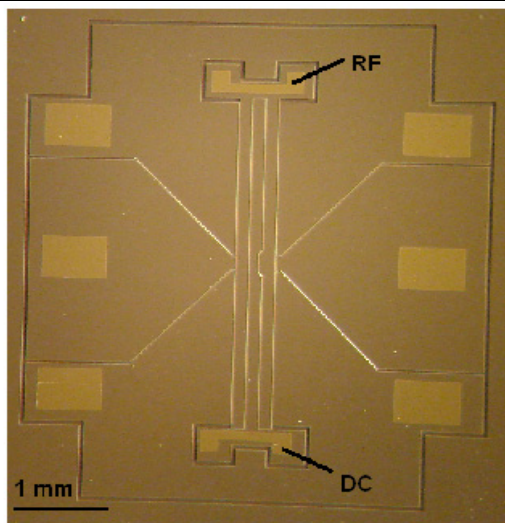
Y. Ge, E. Dauler, J. Labaziewicz, S. Wang, I. Chuang, K. K. Berggren

We demonstrate an approach for fabricating a superconducting surface-electrode ion trap. Surface-electrode ion traps, while promising for large-scale quantum computation, have long been challenged by ion heating rates, which increase rapidly as trap length scales are reduced [1,2,3]. One promising approach to solve this problem is to fabricate trap electrodes from superconductors, and to operate the ion trap chip at cryogenic temperatures.

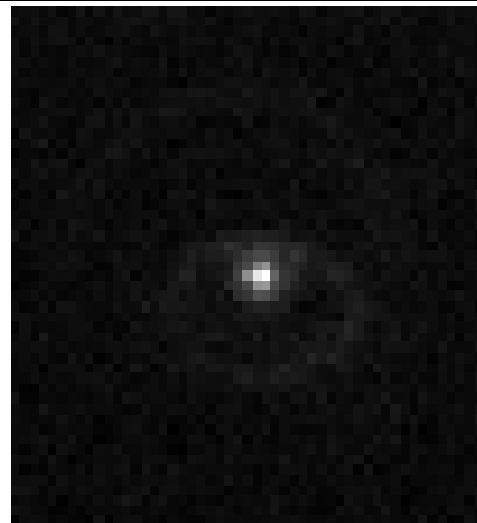
The surface-electrode superconducting ion trap was fabricated from 140-nm-thick NbN on an insulating sapphire substrate. As shown in Figure 1, the ion trap has one RF, one ground and four DC electrodes. Ions are trapped 100  $\mu\text{m}$  above the surface in the center of the central ground electrode [4]. The NbN was deposited on R-plane sapphire using DC magnetron sputtering of a Niobium target in a 12% N<sub>2</sub> + 88% Ar gas mixture. Before deposition, the wafer was backside-coated with Niobium and the wafer was heated on an 800°C inconel block during the NbN deposition. The resulting ~140-nm-thick NbN film was superconducting at temperatures below  $T_c = 13\text{K}$ . In order to define the electrodes, optical lithography was performed using negative photoresist (NR9-3000) and this pattern was transferred into the 140-nm-thick NbN film using

reactive-ion-etching with CF<sub>4</sub> and O<sub>2</sub>. Finally, gold contact pads were defined by optical lithography using positive photoresist (S1813) and a liftoff process. To preserve superconductivity, all baking procedures were performed at or below 90°C.

The superconducting NbN ion trap successfully trapped single ions at temperatures sufficiently below its critical temperature, where the superconductivity could be maintained while applying the required trapping voltages. We measured the ion heating rates while operating the superconducting NbN ion trap at 6K. A single Strontium ion was sideband cooled to its quantum ground state motion, as shown in Figure 2. One 100 μm size superconducting NbN ion trap showed an ion heating rate of 10~20 quanta/s, similar to low-resistivity, non-superconducting ion traps at cryogenic temperatures. When the temperature was above T<sub>c</sub>, the NbN ion trap failed to trap ions due to the large resistivity change of the NbN RF electrode around T<sub>c</sub>. In the future, superconducting traps with lower normal-state resistivity will be investigated in order to study how the electrode resistivity influences the ion heating rate.



**Figure 1:** Optical microscope photograph of a surface electrode NbN ion trap with gold contact pads. The ion trap consists of one RF, one Ground and four DC electrodes.



**Figure 2:** A single Strontium ion is trapped with the surface electrode NbN ion trap at 6K, sideband cooled to its quantum ground state motion.

#### References:

- [1] D. Stick, W. K. Hensinger, S. Olmschenk, M. J. Madsen, K. Schwab and C. Monroe, "Ion trap in a semiconductor chip," *Nature Phys.* 2: 36-39 (2006).
- [2] L. Deslauriers, S. Olmschenk, D. Stick, W. K. Hensinger, J. Sterk, and C. Monroe, "Scaling and Suppression of Anomalous Heating in Ion Traps," *Phys. Rev. Lett.* 97: 103007 (2006).
- [3] S. Seidelin and J. Chiaverini, " Microfabricated Surface-Electrode Ion Trap for Scalable Quantum Information Processing," *Phys. Rev. Lett.*, 96:253003 (2006).
- [4] Jaroslaw Labaziewicz, Yufei Ge, Paul Antohi, David Leibbrandt, Kenneth Brown, and Isaac L. Chuang, " Suppression of Heating Rates in Cryogenic Surface-Electrode Ion traps," *Phys. Rev. Lett.* 100: 130001 (2008).

## 2. Packaging superconductive nanowire single-photon detectors

### Sponsors:

IARPA

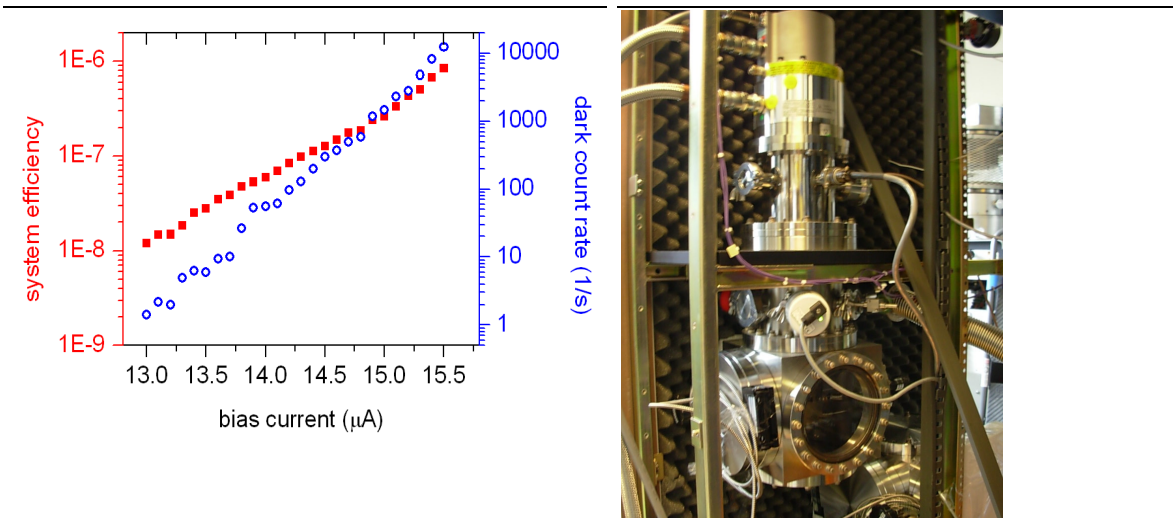
### Project Staff:

X. Hu, F.N.C. Wong, K.K. Berggren

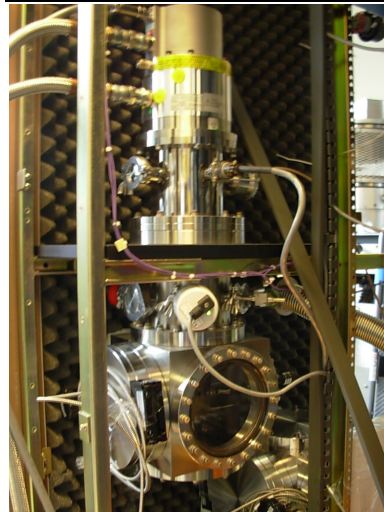
Superconductive nanowire single-photon detector (SNSPD) is an emerging ultra-sensitive photon counting technology which can be used in quantum key distribution, deep space optical communication and defect-detection for integrated circuits. In the past, we have successfully developed a robust process to fabricate SNSPDs and have demonstrated device detection efficiency above 50% at near infrared wavelengths.[1] To enable the above-mentioned applications, however, one remaining challenge must be met – packaging the SNSPDs so that the light can be efficiently coupled into the detectors. This step is difficult because of the small active area of the SNSPD and its low temperature operation.

To achieve such efficient coupling, we have designed an experimental setup to perform helium-immersed testing of SNSPDs inside a dewar. The major part of the setup is a probe in which are integrated a chip-holder, a fiber-focuser, three nanopositioners, a temperature sensor, and electrical connections. The fiber-focuser is used to shrink the spot-size of the light from a single-mode fiber down 5  $\mu\text{m}$ , and the nanopositioners are used to accurately adjust the position of the spot in-situ three-dimensionally. The detector is directly connected with an SMA connector through wire bonding. Some preliminary results are shown in Figure 1, and further optimization is being performed.

Meanwhile, a more convenient, plug-in SNSPD system is being developed based on a closed-cycle, two-staged cryocooler which can reach 2.8 K (see Figure 2). Its main parts include a two-stage cold head, a compressor, a pump system and a vacuum chamber. The main advantage of the cryocooler over the dewar is that it does not need liquid helium, and is free to move. Therefore, this SNSPD system can facilitate many experiments in the field of quantum optics.



**Figure 1:** System efficiency and dark count rate of a single-photon detector measured by helium-immersion testing.



**Figure 2:** The two-stage cryocooler for the testing of superconductive nanowire single-photon detectors.

**References:**

- [1] K.M. Rosfjord, J.K.W. Yang, E.A. Dauler, A.J. Kerman, V. Anant, B.M. Voronov, G.N. Gol'tsman, and K.K. Berggren, "Nanowire single-photon detector with an integrated optical cavity and anti-reflection coating," *Optics Express* 14 (2): 527-534 (2006).

**3. Optimum Exposure Parameters for High-Resolution Scanning Electron Beam Lithography**

**Sponsors:**

NRI, KAUST, MIT

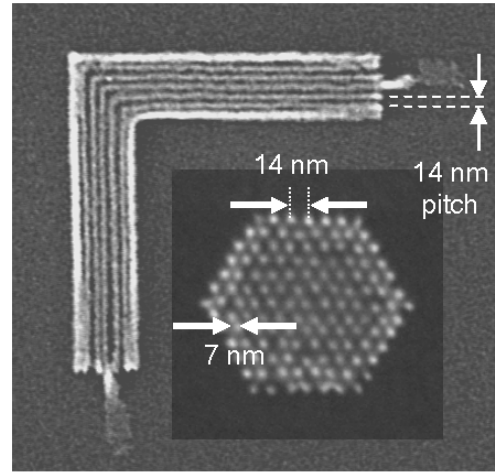
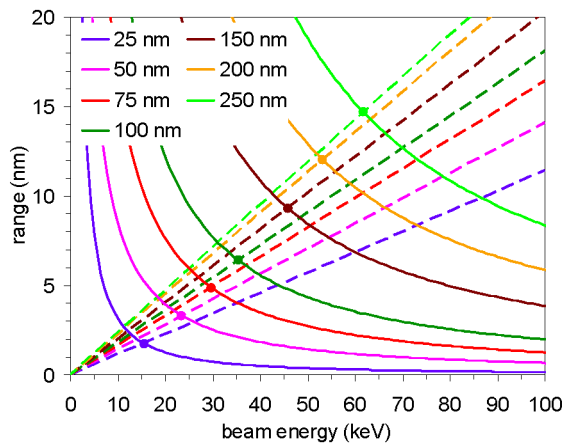
**Project Staff:**

B. Cord, J. Yang, K.K. Berggren

The resolution of a scanning electron beam lithography (SEBL) exposure process is primarily limited by two processes: (1) the range of forward scattering of the incident beam; and (2) the range of secondary electrons produced by interactions between the primary beam and the resist.<sup>1,2</sup> The forward scattering behavior has been well-characterized, and its extent is known to be proportional to the resist thickness and inversely proportional to the primary beam energy.<sup>3</sup> The behavior of the secondary electrons is less well-documented, but their approximate range is thought to be independent of resist thickness and either independent of<sup>2</sup> or weakly proportional to<sup>4</sup> the primary beam energy.

The dependencies of these two limiting factors suggest that, for a given resist thickness, there exists a "crossover" energy where the process is balanced between the forward-scattering- and secondary-electron-limited regimes and further increase in the beam energy does not result in increased resolution. While it has been hypothesized that secondary-electron range is the main resolution limiter in most thin-resist applications<sup>1</sup>, the energies at which forward scattering becomes irrelevant have never been determined.

Using Monte Carlo simulations<sup>5</sup>, we have calculated both the forward scattering length and average secondary electron range over a range of beam energies and resist thicknesses (figure 1). The results suggest that, for resists thinner than 100 nm, the crossover beam energy occurs at approximately 30-40 keV, suggesting in turn that thin-resist lithographic resolution on relatively low-cost 30 keV SEBL tools may be equal or superior to that attainable on high-end, high-beam-energy systems. This hypothesis is partially supported by the micrographs in figure 2, which demonstrate sub-10-nm lithographic resolution in 35-nm-thick films of HSQ<sup>6</sup> using MIT's 30 keV Raith-150 SEBL tool.



**Figure 1:** Curve fits of Monte Carlo results for the forward scattering length  $\alpha$  (solid lines) and the secondary electron range  $\lambda$  (dashed lines) as a function of beam energy for various resist thicknesses. The crossover points, indicating the beam energy at which the resolution is maximized, are marked with dots.

**Figure 2:** 7-nm-wide nested “L” and dot (inset) features on a 14 nm pitch, exposed in 35 nm of HSQ at 30 keV using the Raith-150 SEBL tool at MIT.

#### References:

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- [2] D. C. Joy, Microelectron. Eng. 1, 103-119 (1983).
- [3] R. J. Hawryluk, J. Vac. Sci. Technol. 19(17) (1981).
- [4] M. Bolorizadeh and D. C. Joy, J. Micro./Nanolith. MEMS MOEMS 6(2) (2007).
- [5] P. Hovington, D. Drouin, and R. Gauvin, Scanning 19(1), 1-14 (1997).
- [6] J. K. W. Yang and K. K. Berggren, J. Vac. Sci. Technol. B 25(6), 2025-2029 (2007).

#### 4. High Resolution Nanoimprint Lithography

##### Sponsors:

King Abdullaziz City of Science and Technology (KACST), MIT.

##### Project Staff:

D. Morecroft, J. K. W. Yang, K. K. Berggren: Quantum Nanostructures and Nanofabrication Group, Research Laboratory of Electronics, MIT

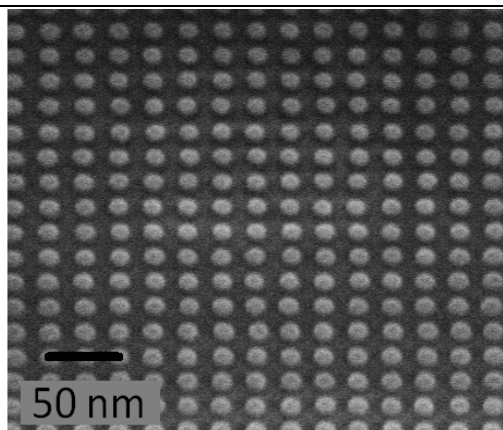
Q. Xia, W. Wu and R. S. Williams: Hewlett-Packard Laboratories

Nanoimprint lithography (NIL) is quickly maturing as a next-generation patterning technique that offers the combined advantages of high resolution, low cost and high throughput [1]. Unlike conventional optical lithography techniques, NIL physically imprints a 3D-structured mold into

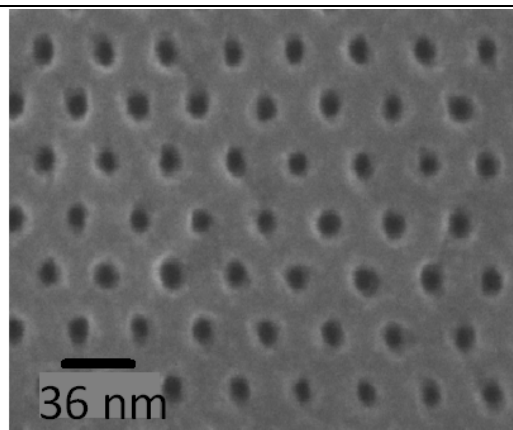
resist. The mold imprints the inverse pattern, which can then be transferred into the substrate by reactive ion etching. While nanoimprint lithography is attractive as a low-cost high throughput technique, the fabrication of its imprint mold still depends on other lithography methods. A key issue to resolve is the ultimate pitch resolution of the patterns since this determines the upper limit of the density. In this work we combine the high resolution capabilities of electron beam lithography with the high throughput of nanoimprint to obtain densely packed nanostructures over a large surface area.

Previously results have shown that negative tone resist can be used in combination with a salty developer technique to enhance contrast [2]. Using this technique, hydrogen silsesquioxane (HSQ) resist was spun onto silicon substrate with a thickness of 20 nm, and electron-beam lithography was carried using a Raith 150 EBL tool with a 30 kV acceleration voltage. The patterns were developed in an aqueous solution of 1% NaOH, 4% NaCl, and pattern transfer into the silicon was carried out using reactive ion etching in a Plasma Therm 770 with a HBr plasma. Fig. 1 shows a tilted scanning electron micrograph of 25 nm pitch square-packed dots after reactive ion etching with a depth profile of 35 nm. The results show good profile transfer between the HSQ and silicon. The patterned silicon substrate was then used as a mold for nanoimprint lithography, and Fig. 2 shows a 36 nm pitch hexagonal dot array successfully transferred into the nanoimprint resist.

There are many potential applications for this patterning process, for example nanopatterned electrodes for fuel cells and batteries where the increased surface area may enhance the catalytic activity.



**Figure 1:** Tilted scanning micrograph of 25 nm pitch pillars after reactive ion etching with a hydrogen bromide plasma into the silicon substrate.



**Figure 2:** Scanning electron micrograph of 36 nm pitch dots imprinted into nanoimprint resist with 4 nm Ti for imaging.

#### References:

- [1] S. Y. Chou, P. R. Krauss, and P. J. Renstrom, "Imprint Lithography with 25 nm Resolution", *Science*, vol. 272, pp. 85–87, 1996.
- [2] J. K. W. Yang, K. K. Berggren, "Using High Contrast Salty Development of Hydrogen Silsesquioxane for Sub-10 nm Half Pitch Lithography", *J. Vac. Sci. Technol. B*, vol. 25(6), pp. 2025, 2007.

## 5. Templated Self-Assembly of sub-10nm Quantum Dots

### Sponsors:

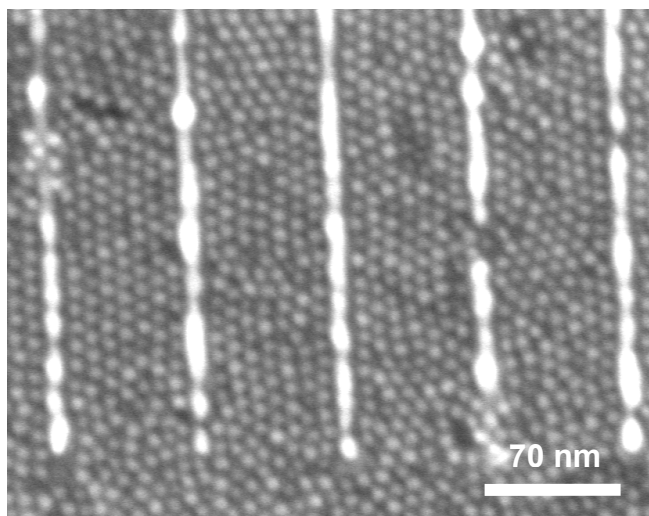
MARCO MSD, NRI, and IBM

### Project Staff:

J. Leu, B. Cord, P. Anikeeva, J. Halpert, V. Bulovic, K. Berggren

Patterned templates can guide the self-assembly of nanoparticles into ordered arrays [1]. Our motivation in pursuing templated self-assembly is to develop a robust method for the creation of ordered structures at length scales below ten nanometers. The basic process entails creating surface relief templates via electron-beam lithography, and spin-coating a suspension of colloidal nanoparticles onto the template. As the solvent evaporates, the quantum dots self-assemble primarily through the capillary forces created by the dewetting of the template [2].

We demonstrate this technique at sub-10nm length scales by spin-coating a solution of organically-capped CdZnS semiconducting quantum dots onto nanopatterned grating structures on silicon substrates. We observe the geometric confinement of the quantum dots via physical templating and capillary forces into well-ordered monolayer aggregates with defined lattice orientations. While recent research has demonstrated the ability to self-assemble sub-10nm metallic nanoparticles via capillary forces into physical templates of similar size [2], this work is unique in the demonstration of lattice orientation control via physical templating at sub-10nm length scales.



**Figure 1:** Scanning electron micrograph of a self-assembled quantum dot monolayer on a templated silicon substrate. The vertical lines visible are part of a template grating, with 10-nm-wide, 80-nm-tall Au lines at a pitch of 80 nm. The spheres are organically capped 8 nm CdZnS semiconducting quantum dots.

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**6. Fabrication of Superconducting Nanowire Single-Photon Detectors with High Fill-Factors**

**Sponsors:**

MIT, and AFOSR

**Project Staff:**

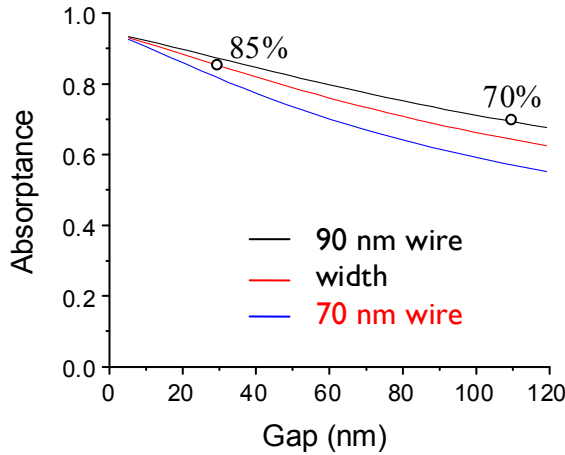
Joel K.W. Yang, Andrew J. Kerman, Vikas Anant, Eric A. Dauler and Karl K. Berggren

In the past, we have fabricated superconducting nanowire single-photon detectors (SNSPDs) with detection efficiencies (DE) as high as 57% at 1550 nm wavelengths [1]. The nanowires in these SNSPDs were 90 nm wide and were separated by 110 nm (i.e. a 45% fill factor) in a meander structure patterned in NbN films. While a 57 % DE is acceptable for many applications, a much higher DE will be valuable (if not necessary) in certain applications such as linear-optics quantum computing and photon number resolution. One approach to increasing the DE of SNSPDs is to increase the optical absorption of the device by increasing the fill factor of the meander structure.

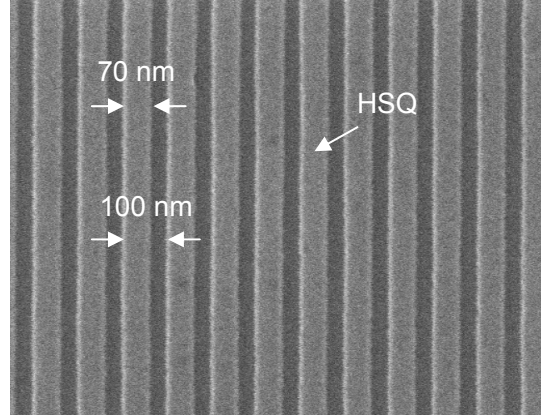
Figure 1 shows numerical calculations of the absorptance in the SNSPD meander structure, indicating that reducing the gap width between wires in the meander can significantly increase photon absorptance and hence the DE. For example, we can predict that by increasing the fill factor from the current value of 45% to 70%, the device DE would increase from 57% to ~70%.

Recently we developed a high-resolution nanofabrication method using a combination of a high-contrast resist process and electron-beam lithography to achieve sub-10-nm nanostructure dimensions [2]. This technique could be used to fabricate SNSPDs with fill factors as high as 80% and wire widths as narrow as 40 nm. Figure 2 shows an example of a grating structure with 70% fill factor that has been fabricated in HSQ resist using this method.





**Figure 1:** Numerical calculations show that the photon absorbance in the SNSPD meander increases with decreasing gap width between the nanowires. Our original SNSPD design of 90 nm wide wire with a 110 nm wide gap has an absorbance of ~70%. However, increasing the fill factor through better lithography to achieve 70-nm-wide wires and a gap width of 30 nm will result in an increase in absorbance to 85% leading to higher detection efficiencies.



**Figure 2:** Top down SEM image of HSQ structures on Si with a fill factor of 70% which could potentially be used for making SNSPDs with higher DE. Schematic for helium-immersion testing of superconducting nanowire single-photon detectors.

#### References:

- [1] K. M. Rosfjord, J. K. W. Yang, E. A. Dauler, A. J. Kerman, V. Anant, B. M. Voronov, G. N. Gol'tsman, and K. K. Berggren, "Nanowire Single-photon detector with an integrated optical cavity and anti-reflection coating," *Optics Express*, vol. 14, pp. 527-534, 2006.
- [2] J. K. W. Yang and K. K. Berggren, "Using high-contrast salty development of hydrogen silsesquioxane for sub-10-nm half-pitch lithography," *Journal of Vacuum Science & Technology*, vol. 25, pp. 2025-2029, 2007.

### 7. Hydrogen Silsesquioxane Nano-posts as Decoys for Guiding the Self-Assembly of Block Copolymers

#### Sponsors:

MIT, NRI, and KACST

#### Project Staff:

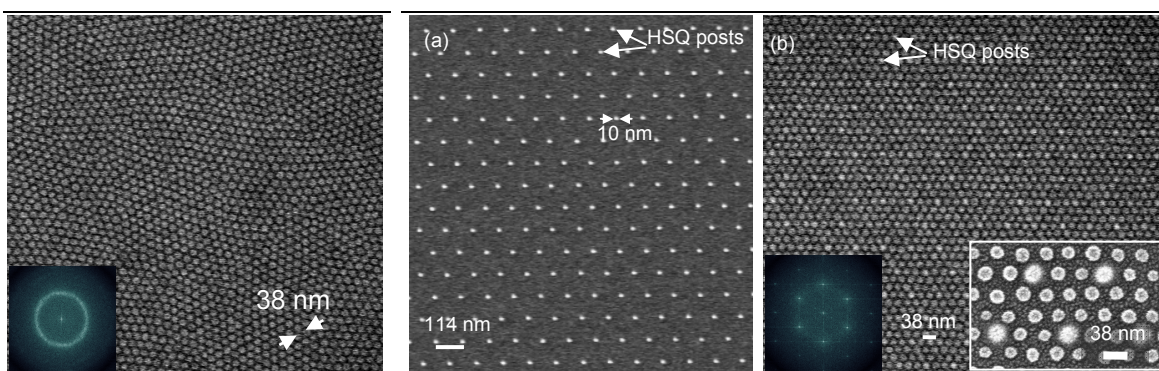
Joel K.W. Yang, Yeon Sik Jung, Ion Bitu, Edwin L. Thomas, C. A. Ross and Karl K. Berggren

According to the International Technology Roadmap for Semiconductors, semiconductor companies are expected to produce memory cells with a half-pitch of 22 nm by the year 2011. Fabricating such small structures is a huge challenge even with today's most advanced photolithography methods. However, the technology for making sub-20-nm nanostructures is already available in the self-assembly of block-copolymers (BCP). This bottom-up technique is scalable to even smaller dimensions by choosing tinier BCP molecules, making it an attractive "next-generation lithography" method for creating dense periodic structures over large areas. Major challenges still remain in (1) the accurate control of the order and position of the

nanostructures, and (2) the formation of arbitrary structures using BCPs. In this work, we focus on solving the first problem.

Fig. 1 shows the randomly oriented, hexagonally-packed nanostructures formed in a BCP film on a flat Si substrate. This pattern was formed after annealing a thin layer of polystyrene-*b*-polydimethylsiloxane (PS-*b*-PDMS) BCP and selective etching of the PS majority block [2].

To induce long-range order in the BCP, we first introduced topography on the flat surface by fabricating a periodic array of posts in hydrogen silsesquioxane (HSQ) resist by electron-beam lithography (see Figure 2a). These posts were ~10 nm in diameter and 35 nm tall and acted as decoys (or substitutes) for single BCP spheres. Figure 2b shows that order and orientation control were achieved when the BCP self-assembled about the array of posts. In contrast to previous work [1] where the topographical structures (e.g. trenches) used for guiding the BCP were large and clearly identifiable after processing, our nano-posts blend-in among the BCP spheres while physically pinning-down the BCP lattice position in 2D.



**Figure 1:** SEM image of randomly oriented spheres formed by BCP self-assembly on a flat surface. The fourier transform (inset) shows a circular halo characteristic of randomly oriented grains

**Figure 2:**(a) SEM image of a periodic array of 35-nm-tall, 10-nm-diameter HSQ posts fabricated by electron-beam lithography and developed in a high-contrast salty developer [3]. (b) Ordered packing of BCP spheres guided by the lattice of HSQ posts. HSQ posts blend-in with the BCP spheres but are visible as slightly brighter dots in the image and bottom-right inset. The fourier transform (left inset) shows an arrangement of bright spots characteristic of a hexagonally packed crystal.

By adjusting the lattice spacing of the HSQ posts, different BCP packing orientations formed that were commensurate with the HSQ lattice. We therefore have control over the packing order and orientation of the BCP spheres. The resultant PDMS and HSQ nanostructures were etch resistant and could be used for pattern transfer into underlying functional materials such as magnetic films for high-density data storage applications.

#### References:

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- [2] Y. S. Jung and C. A. Ross, "Orientation-controlled self-assembled nanolithography using a polystyrene-polydimethylsiloxane block copolymer," *Nano Letters*, vol. 7, pp. 2046-2050, 2007.

- [3] J. K. W. Yang and K. K. Berggren, "Using high-contrast silsesquioxane for sub-10-nm half-pitch lithography," *Journal of Vacuum Science & Technology*, vol. 25, pp. 2025-2029, 2007.

## 8. Scanning-Electron-Beam Lithography (SEBL) Facility

### Sponsors:

MIT Institute Facility under RLE

### Project Staff:

Mark K. Mondol, Dr. Feng Zhang, Prof. Henry I. Smith, Prof. Karl Berggren

In 2004, the Nanostructures Lab converted its scanning-electron-beam-lithography (SEBL) facility in Room 38-165 into an Institute-wide service facility under the Research Laboratory of Electronics (RLE). This facility provides MIT and outside users with easily accessible e-beam lithography, coupled with resident expertise and advice. The facility is managed by Mark Mondol who provides training on the e-beam tools, direct patterning service, and advice on optimal nanofabrication techniques and strategies. The NanoStructures Laboratory (NSL) and the Microsystems Technology Laboratories (MTL) have service facilities for spin coating of resists, resist development and other forms of processing.

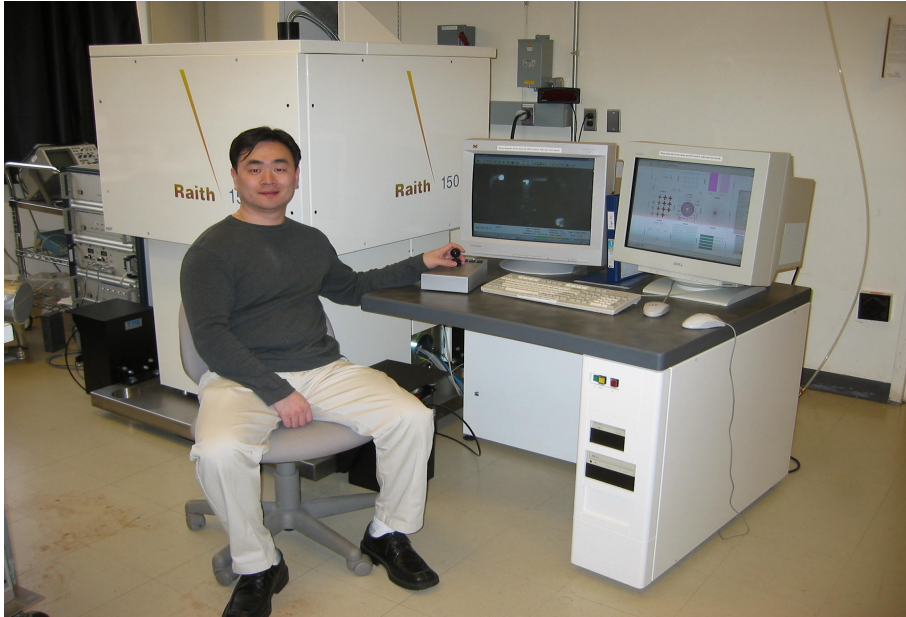
Projects that made use of the SEBL facility during the past year included: patterned nanotube growth; relief templates for self assembly of block copolymers; point-contact devices; 1-D and 2-D photonic crystals; ring-resonator add/drop filters; optical-polarization splitter-rotator devices; novel liquid-crystal devices; magnetic-memory devices; quantum photodetectors; templates for nanoimprint lithography; photomasks for interferometric-spatial-phase-imaging alignment and gapping; 4-point contacts for measurements on nanotubes and nanowires; III-V compound T-gate HEMTs and arrays of Fresnel zone plates. Research in lithographic processing included extreme cold development of PMMA and novel developer solutions for HSQ which demonstrated improved resolution and contrast. Use of the facility, by the MIT community, was widespread, there were: 25 Principal Investigators, 7 Departments, 8 Labs or Centers, 2 non-MIT entities and 45 distinct trained users over the last year.

Two SEBL tools are available. The Raith Turnkey 150 system is shown in Figure 1. Its electron-optical column is essentially identical to that of a Zeiss Gemini SEM, and provides a beam diameter as fine as 2 nm. Linewidths of  $\leq 9$  nm have been written with the system, as illustrated in Figure 2. The Raith 150 includes a pattern generator and laser-interferometer-controlled stage with an integrated software package which was upgraded to version 4.0 in the past year. This upgrade improved writing speed and system stability. Version 4.0 software now allows users to do automated field alignment to approximately  $\pm 25$ nm. The system can operate from 1 to 30keV accelerating voltage. Wafers up to 150 mm can be loaded into the system. Typically, users are trained for 3 to 10 hours and then allowed to operate the tool on their own. The tool is available, for most users, 24 hours a day, 7 days a week.

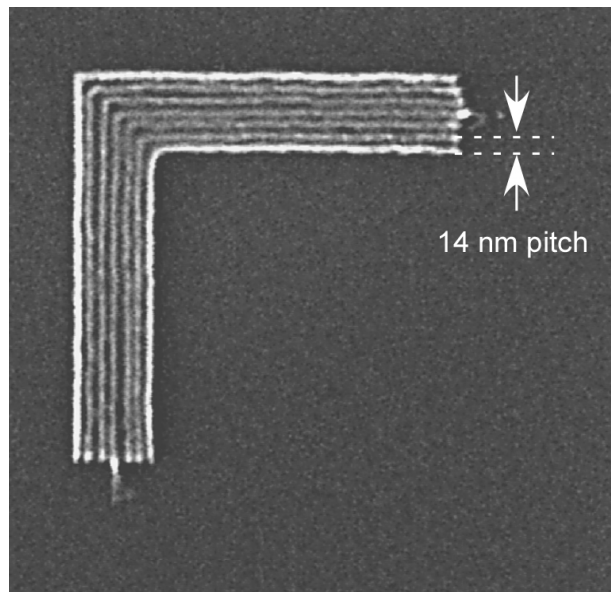
Figure 3 is a photograph of the VS-26 system. This instrument was put together at MIT from two systems (VS-2A and VS-6) obtained as gifts from IBM in the mid 1990's. VS-26 has a minimum beam diameter of about 10 nm. It operates at a fixed accelerating voltage of 50keV. Conversion software has been developed which allows a CAD data file to be fractured and translated prior to exposure, additional software was developed to generate arbitrary arcs. Substrates up to 200 mm diameter can be exposed at linewidths down to  $\sim 30$  nm. However, the area available for patterning is limited to 95x95 mm.

The Raith 150 is used in a program to develop spatial-phase-locked e-beam lithography, described elsewhere. The objectives of that program are to achieve sub-1 nm pattern-placement

accuracy, and to reduce the cost and complexity of SEBL. In a conventional SEBL system costing several million dollars, pattern placement accuracy is typically much worse than 10 nm. The SEBL facility encourages users with a variety of experience levels and requirements. Experienced users are able to carry out complex, multilevel aligned exposures on the Raith-150 tool. Less experienced users get hands-on instructions from facility staff, and guidance during the learning and initial fabrication stages.



**Figure 1.** The Raith-150 electron-beam lithography system. This tool provides sub-20-nm patterning resolution, and pattern-placement accuracy  $\sim 1\text{nm}$  via spatial phase locking. The operator is Dr. Feng Zhang.



**Figure 2:** Scanning-electron micrograph of exposed and developed HSQ illustrating the resolution of the Raith 150 SEBL system. (J. K. W. Yang and K. K. Berggren, "Using High-Contrast Salty Development of Hydrogen Silsesquioxane for Sub-10-nm-Half-Pitch Lithography," *Journal of Vacuum Science & Technology B*, submitted for publication (2007))





**Figure 3.** Photograph of the VS-26 scanning-electron-beam lithography system.

## Publications

### Journal Articles, Published

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