Integrated Systems

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Introduction

Integrated Systems Group is focused on several key design aspects of modern integrated systems. The group is focused on building cutting edge, energy-efficient integrated systems through vertical optimization encompassing communications and signal processing algorithms and architectures, and digital and mixed-signal circuits. The main research topics include circuit and system design for on-chip and off-chip interconnects, circuit optimization and design methodology, modeling of noise and dynamics in circuits and systems, application of convex optimization to digital communications, analog and VLSI circuits.

Most integrated systems today are limited by tight power and/or throughput constraints. In this environment, the usual system hierarchy becomes inefficient and novel vertical system design approaches are needed to create overall most efficient integrated systems. We believe that this can be achieved by blurring of the strict hierarchy boundaries and modification of standard communication techniques and circuits to perform the operations in a most energy-efficient way.
Some of the example systems that we are interested in are high-speed electrical and optical interfaces, silicon-photonics, metrology for carbon-nanotubes, on-chip signaling and networks, joint circuit and system optimization of a high-speed link, clock generation and distribution for system-on-a-chip.

1. Pre-distorted Charge-Injection Pre-emphasis Transmitter and Trans-impedance Terminated Receiver for Energy Efficient On-Chip Equalized Interconnect

Sponsors
Interconnect Focus Center (IFC), Intel Corporation, Center for Integrated Circuits and Systems (CICS) at MIT, Semiconductor Research Corporation Program and Trusted Foundry.

Project Staff
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This work presents improvement of energy efficiency of equalized-interconnect by proposing two circuit techniques: 1) pre-distorted charge-injection (CI) feed-forward equalization (FFE); 2) trans-impedance (TIA) termination at receiver. Instead of using traditional analog subtraction, CI-FFE injects pre-computed the current value required for FFE into the channel while mitigating the nonlinearity of the driver. The non-linearity of the driver is statically compensated by pre-distorting FFE coefficients. The trans-impedance amplifier terminated at the receiver improves the bandwidth, signal amplitude, and reduces bias current.

A test-chip is fabricated in 90nm CMOS process and consumed about 0.4pJ/b running at 4Gb/s with vertical eye opening about 100mV and horizontal eye opening 50%UI differential peak-to-peak [1].

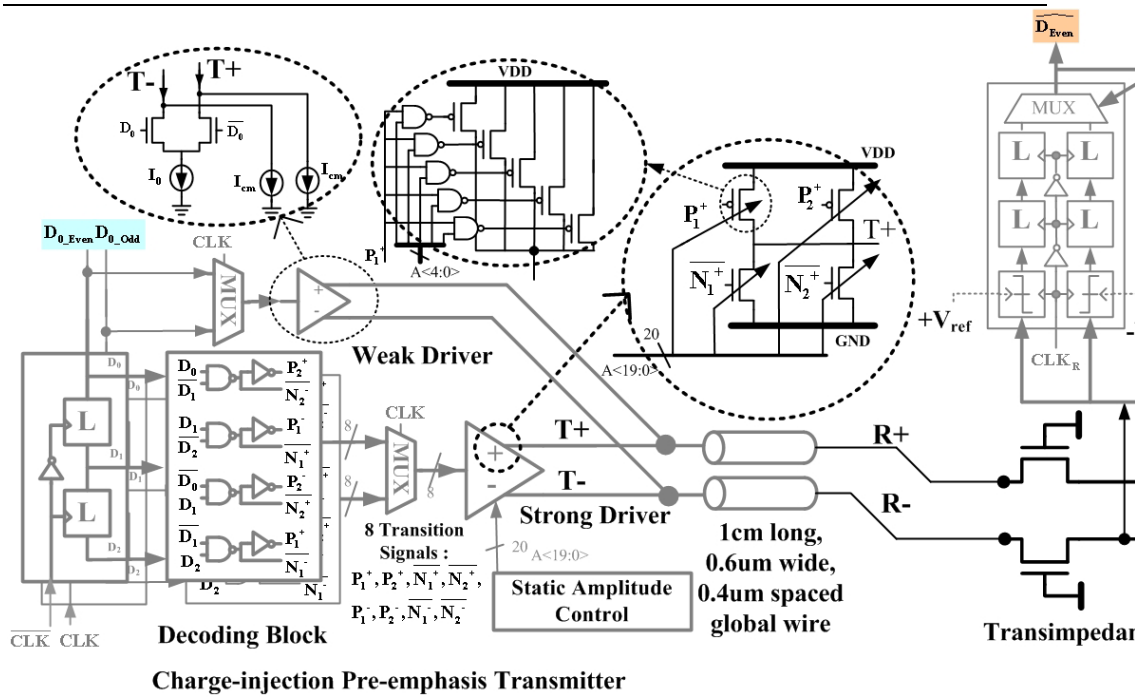

Figure 1: Link Architecture.

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2. A Fractionally Spaced Linear Receive Equalizer with Voltage-to-Time Conversion

Sponsors
National Semiconductor Corporation, CICS

Project Staff
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Based on voltage-to-time conversion technique 00, a pseudo differential two-way-interleaved adaptive linear receive equalizer with two 2x-oversampled feed-forward taps has been designed in a 90 nm CMOS process. It integrates equalization and phase interpolation functions into one unit to simultaneously address inter-symbol-interference (ISI) cancellation and phase synchronization in a link receiver.

Due to the process speed limitation, half-rate time interleaving technique is also applied, Fig. 1. Four sampling phases (Φ_1- Φ_4) with 25% duty cycle are generated locally from Φ and Φ_ and

another pair of quadrature clocks. A voltage-to-time (V2T) block converts the sampled signal into a delayed digital signal, transferring the sampled information into time-domain. All four V2T converters are followed by a time-to-voltage (T2V) stage to realize summing, subtraction and multiplication. Equalizer tap weights are implemented as two programmable reference currents I_1, I_2 biasing T2V blocks. Two slicers with tunable thresholds are added to sense the signs of the input signal and output error of the FSE, respectively, and enable tap weight adaptation with external adaptive engine. The design is fabricated in a 90 nm CMOS process. It operates at 4 Gbps with 8 mW power consumption, and linearity of 4.3 effective bits at 1.2 V supply.

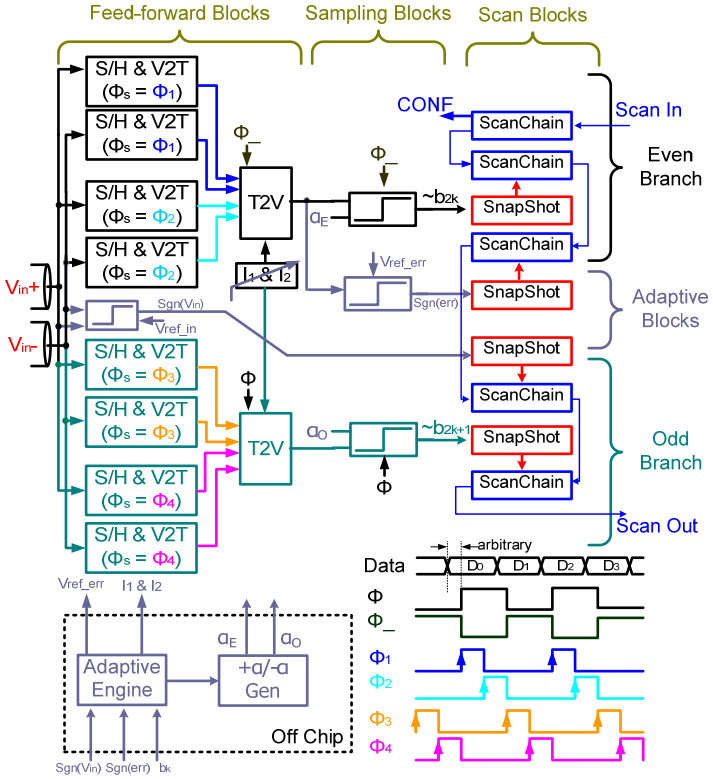

Figure 1. Block diagram of 2-tap 2xoversampled two-way time interleaved architecture. Scan-chain and snapshot are applied for in-situ link characterization.

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3. A Fractionally Spaced Linear Receive Equalizer with Voltage-to-Time Conversion

Project Staff

Wei An and Prof. Vladimir Stojanović

Sponsors

NSF

Reed-Solomon (RS) codes have found widespread application in data storage and communications because of the simplicity of their decoding algorithm. RS codes are also

maximum distance seperable (MDS) codes which meet the Simpleton bound. The first decoding algorithm for RS codes was constructed by Peterson, which was then simplified by Bellerkemp and Massey [1]. A breakthrough by Sudan in 1997 made it possible to decode RS codes beyond half the minimum distance [2]. Backtracking to 1972, Chase [3] developed an efficient *bounded distance decoding* technique that works with any code (that has an efficient *hard decision decoder*). Bellardo and Kavcic [4] observed that for RS codes, both Sudan's and Chase's techniques could be effectively combined, and showed that it is possible to implement a Chase decoder with lower complexity than even the Bellerkemp-Massey decoder. This is known as the Low Complexity Chase (LCC) decoder.

We further improve the decoder performance while reducing its complexity by introducing tree pruning concept. We also implement the decoder using 90nm IBM 9SF technology. We focus on the long code RS [255, 239, 17] and the short code RS [31,25,7]. With the implemented decoders, we investigate relationship between the decoder BER performance the power consumption. The comparison can be made in the framework of LCC vs conventional RS decoder and long vs short decoders.

In the end, we'll understand the improvement of LCC decoder in terms of BER performance, die area and power consumption.

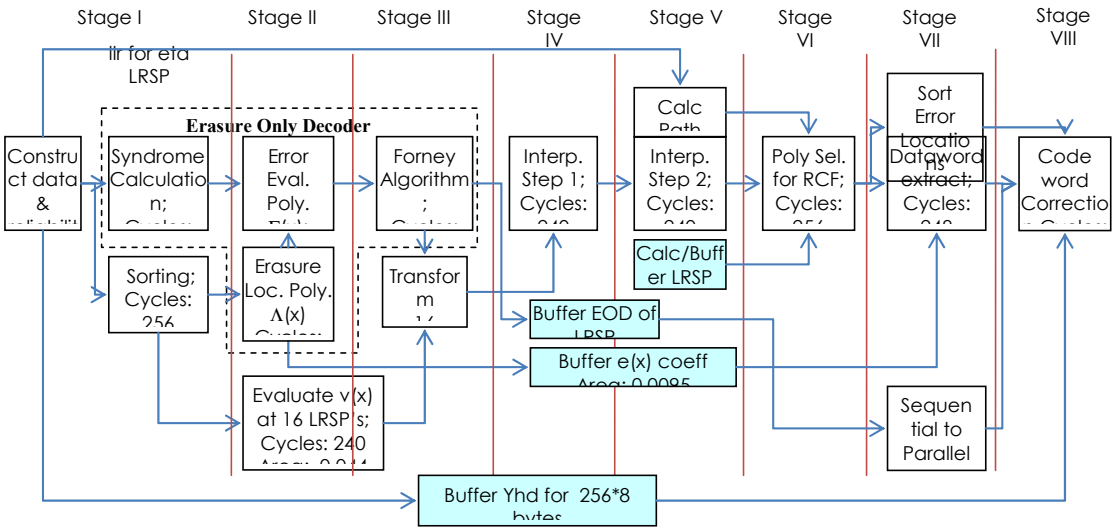

Figure 1: Decoder architecture.

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