Japanese Journal of Applied Physics **50** (2011) 070114
DOI: 10.1143/JJAP.50.070114

High Frequency Performance of Graphene Transistors Grown by Chemical Vapor Deposition for Mixed Signal Applications

Allen Hsu, Han Wang, Ki Kang Kim, Jing Kong, and Tomás Palacios

Massachusetts Institute of Technology, 32 Vassar Street, Cambridge, MA 02139, U.S.A.

Received January 5, 2011; revised March 3, 2011; accepted March 3, 2011; published online July 20, 2011

This paper demonstrates high frequency performance of graphene transistors grown by chemical vapor deposition on copper foils. Using Ti/Pd/Au-based ohmic contacts and a hybrid gate dielectric stack of 5 nm SiO_2 and 15 nm Al_2O_3 grown by atomic layer deposition, graphene transistors with an extrinsic current-gain cut-off frequency (f_T) of 2 GHz and power-gain cut-off frequency, f_{max}, of 5.6 GHz were obtained for a gate length of L_g = 1.6 μm. By applying a bias to the Si substrate the access resistances are reduced, which improved the f_T and f_{max} in the devices to 3.5 and 6.5 GHz, respectively. Finally we demonstrate these devices in a real-application circuit for binary-phase shift keying.

1. Introduction

Graphene is a two-dimensional material of sp^2-bonded carbon atoms. Due to its structure and the high symmetry of the hexagonal arrangement of its atoms, graphene yields many unique and interesting electronic properties including carrier mobilities in excess of 100,000 $cm^2\,V^{-1}\,s^{-1}$ and excellent carrier confinement.[1)] In addition, its unique ambipolar transport enables several novel circuit applications for frequency multiplication, logic inverters, and binary phase shift keying.[2–5)]

Currently, graphene can be obtained from at least three different sources: Highly oriented pyrolytic graphene (HOPG), SiC sublimation, and chemical vapor deposition (CVD) on metal catalysts.[6–9)] Only the later two are viable for large scale integration and only epitaxial SiC has demonstrated RF performance on Si-face.[10,11)] In this material, an intrinsic current-gain cut-off frequency, f_T, of 100 GHz has been reported on graphene transistors with a gate length (L_g) of 240 nm. Unfortunately, the high cost of SiC substrates seriously limits the use and scalability of these devices. CVD Graphene, on the other hand, is grown on relatively inexpensive nickel or copper foil. The graphene is then released by etching the catalyst metal, which creates a free standing graphene film that can be transferred to any arbitrary substrate, including plastics, Si and textiles. 30-in. roll-to-roll processing has already been demonstrated with CVD graphene;[12)] however unique problems related to metal catalyst etching and transfer have limited copper CVD for RF electronic devices.

In this work we demonstrate RF measurements of graphene devices fabricated on CVD-grown graphene. Transistors with a gate length of 1.6 μm showed a maximum extrinsic f_T of 2 GHz. The application of a substrate bias reduces the access resistances and increases the f_T to 3.5 GHz. The effect of scaling the drain-to-source distance (L_{ds}) and gate length (L_g) have also been analyzed. These devices are then used in graphene circuits to demonstrate binary phase shift keying (BPSK).

2. Graphene Synthesis and Transistor Fabrication

The graphene films used in this work were grown by CVD on copper substrates as described in ref. 9. Copper foils are first annealed at 1000 °C in H_2 to remove native oxides and improve surface morphology and then CH_4 is added under low-pressure conditions (300–500 mTorr) to initiate graphene growth. After growth, a protective poly(methyl methacrylate) (PMMA) coating layer is applied on top of the graphene film. The Cu foil is etched first in commercially available copper etchant, then in diluted HCl, and finally washed in deionized water (DIW):H_2O to reduce doping and tearing caused by the metal etchants. Films are then transferred onto polished Si wafers with a 300 nm thermally-grown SiO_2 on top. Prior to the graphene deposition, the wafers undergo RCA clean and 450 °C forming gas anneal to clean the substrate and make it hydrophobic.

The fabrication of graphene transistors starts with the patterning and deposition of the source and drain ohmic contacts. A 2.5 nm Ti/45 nm Pd/15 nm Au metal stack is then deposited by e-beam evaporation and the ohmic contacts are patterned by lift-off. Device isolation is achieved by etching the graphene between devices with an O_2 plasma at 10 mtorr and 100 W RF Power for 30 s. The gate dielectric is formed by depositing 5 nm of SiO_2 by e-beam evaporation and 15 nm of Al_2O_3 deposited using atomic layer deposition (ALD). A 30 nm Ni/200 nm Au/50 nm Ni metal stack is used as the gate metal.

The intrinsic carrier mobility before gate dielectric deposition was measured through Hall measurements on van der Pauw (VdP) structures for a current level of 0.1 mA and a magnetic field of ~0.3 T. These measurements revealed a residual hole carrier concentration of $(5 \pm 3) \times 10^{12}\,cm^{-2}$ with an average mobility of $2000 \pm 500\,cm^2\,V^{-1}\,s^{-1}$. The residual doping is mainly from the metal catalyst and etching/transfer residues. The variation in mobility is largely due to delaminations and tears seen during fabrication and transfer for larger Hall structures. Using back-gated Hall measurements, we extract a mobility dependence on carrier density following $\mu \sim n_s^{-0.57}$. This dependence is characteristic of short range scatters such as point defects, which suggests that reducing intrinsic defects and grain boundaries can lead to even higher mobilities on CVD graphene.[13)]

3. Transistor Characterization

3.1 DC characterization

The DC performance and structure of a typical graphene transistor with a channel width (W) of 25 μm is shown in Fig. 1. The maximum extrinsic DC transconductance, g_m, is 84.3 mS/mm, which corresponds to an extrinsic mobility ($\mu_{FET} = g_m L_{ds}/C_{ox} V_{ds}$) of $146\,cm^2\,V^{-1}\,s^{-1}$ given a measured gate capacitance (C_{ox}) of 2.1 $fF/\mu m^2$. Hall measure-

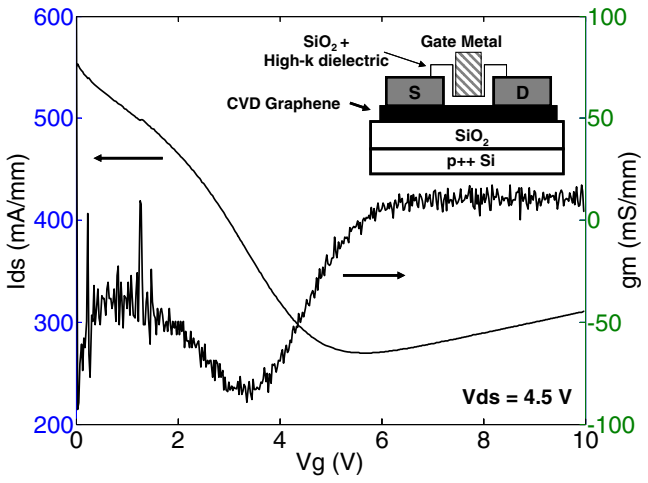


Fig. 1. (Color online) DC characteristics and diagram of a typical graphene device used in this work. The device dimensions are $L_{ds} = 1.7\,\mu m$, $L_g = 1.6\,\mu m$, and $W = 25\,\mu m$. The transistor was measured in vacuum at room temperature.

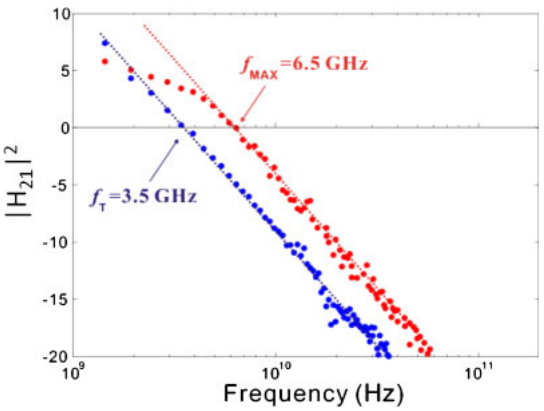


Fig. 2. (Color online) RF characteristics for a GFET with $L_g = 1.6\,\mu m$ and $L_{ds} = 1.7\,\mu m$ with substrate biased at $-50\,V$. The effect of the pad capacitances has been de-embedded. Bias conditions are $V_{ds} = 3\,V$ and $V_{gs} = 1.5\,V$.

ments after gate dielectric deposition estimate the mobility closer to $500\,cm^2\,V^{-1}\,s^{-1}$. The discrepancy between these extraction methods is due to the contact resistance which lowers the current and consequently also the extrinsic DC g_m. Circular TLM measurements estimate contact resistances around 2–5 $k\Omega\,\mu m$ for the ohmic contacts.

3.2 RF characterization

The small signal S-parameters of graphene field-effect transistors (GFETs) were measured at room temperature using a vector network analyzer (Agilent N5230) with line-reflect-match calibration. Figure 2 shows the performance of a typical graphene FET under a bias conditions of $V_{ds} = 3\,V$ and $V_{gs} = 1.5\,V$, the device is in the non-saturated regime. The gate length of the device is $1.6\,\mu m$ and the gate width is $25\,\mu m$. As expected, the $|h_{21}|^2$ plot shows a frequency slope of $-20\,dB/dec$. An extrinsic cutoff frequency (f_T) of 3.5 GHz is extracted after de-embedding the pad capacitances,[14] which yields an extrinsic $f_T \cdot L_g$ of $5.6\,GHz\,\mu m$. The extrinsic g_m calculated from S-parameters was 120 mS/mm. A maximum oscillation frequency (f_{max}) of 6.5 GHz is extracted from Mason's unilateral gain (U), with a slope of $-20\,dB/dec$. These results were obtained with a bias of $-50\,V$ applied to the substrate. The substrate bias is important for significantly improving the RF characteristics of the GFETs. Without substrate bias, the f_T and f_{max} are 2 and 5.6 GHz, respectively, at $V_{ds} = 3\,V$ and $V_{gs} = 1.5\,V$. The effect of the substrate bias is attributed to the improved conductivity in the access region due to the substrate modulation as shown in Table I. The negative substrate bias dopes the graphene p-type thereby reducing the access resistance.

Table I. Effect of substrate bias on small signal access resistances. $V_{ds} = 3\,V$, $V_{gs} = 1.5\,V$.

	$V_{SUB} = 0\,V$	$V_{SUB} = -50\,V$
f_T (GHz)	2	3.5
R_s ($\Omega\,mm$)	5.6	2.2
R_d ($\Omega\,mm$)	6.6	2.3

Table II. Main elements of the small signal equivalent circuit of two graphene transistor with $L_g = 1.6\,\mu m$ and a channel width of $2 \times 25\,\mu m^2$.

Device	V_{ds} (V)	V_{gs} (V)	C_{gs} (pF/mm)	C_{gd} (pF/mm)	$g_{m,ext}$ (mS/mm)	R_s ($\Omega\,mm$)	$f_{T,ext}$
1	3	1.5	3.3	2.5	120	2.2	3.0
2	3	1.5	3.6	2.6	115	2.2	2.8

Table II lists the key elements of the small signal equivalent circuit of the graphene transistor analyzed in Fig. 2. The device parameters are extracted after de-embedding the coplanar-waveguide (CPW) pad capacitances.[14] The total gate capacitance, $C_{gs} + C_{gd}$, of the device varies from 6.1 to 6.7 pF/mm as V_{DS} changes from 2 to 5 V. This is higher than the geometric capacitance of 3.4 pF/mm, estimated using the measured gate capacitance per unit of area ($2.1\,fF/\mu m^2$). The discrepancy in the capacitance value may be due to the effect of fringing field and the close proximity of the source and drain contacts. Using the extracted RF g_m of 120 mS/mm at $V_{ds} = 3\,V$, the extrinsic $f_T = g_{m,ext}/[2\pi \cdot (C_{gs} + C_{gd})]$ is estimated to be 3.0 GHz, in good agreement with the measured value of 3.5 GHz. We note that the RF g_m is larger than the DC g_m, which might be attributed to charge trapping in graphene or gate dielectric defects. The traps cannot respond to the small signal applied to the gate electrode, leading to high g_m.[15] Taking into account the source access resistance, the intrinsic g_m is estimated to be $g_{m,int} = g_{m,ext}/(1 - g_{m,ext}R_s) = 165\,mS/mm$. Hence, the intrinsic f_T of the device is 4 GHz with an intrinsic $f_T \cdot L_g$ of $6.4\,GHz\,\mu m$.

Figure 3 shows the scaling of extrinsic f_T and f_{max} as a function of gate length without substrate bias. Before de-embedding the contact pads, f_T and f_{max} increases from 1 to 1.5 GHz, and from 1.5 to 4.6 GHz, respectively, as the gate length shrinks from 5 to $1.4\,\mu m$. After de-embedding the contact pads, f_T and f_{max} increases from 1.1 to 2.2 GHz, and from 1.5 to 6 GHz. The scaling does not follow the $1/L_G^2$

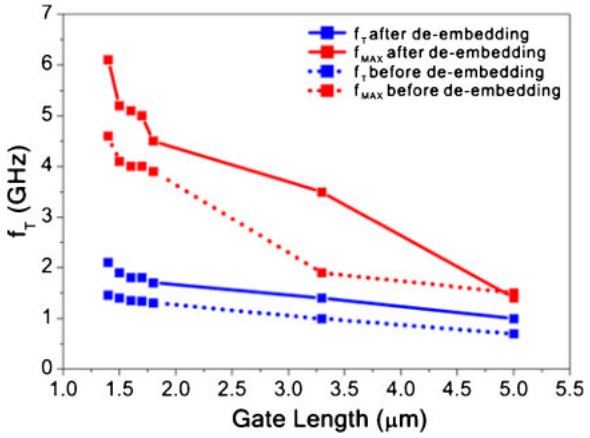


Fig. 3. (Color online) Scaling of extrinsic f_T and f_{max} with gate length. The drain and gate bias conditions were optimized in each device for maximum f_T. No substrate bias was applied to reduce the access resistance in these devices.

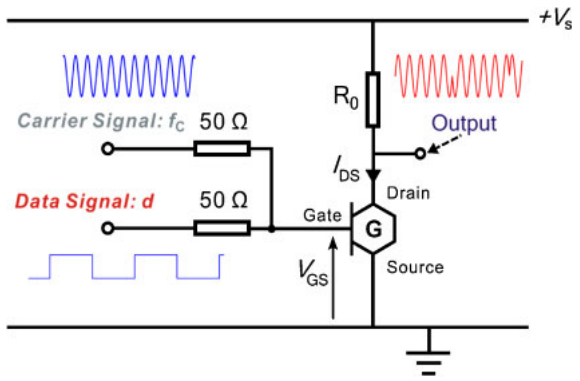


Fig. 4. (Color online) Diagram of a GFET-based binary phase shift keying circuit.

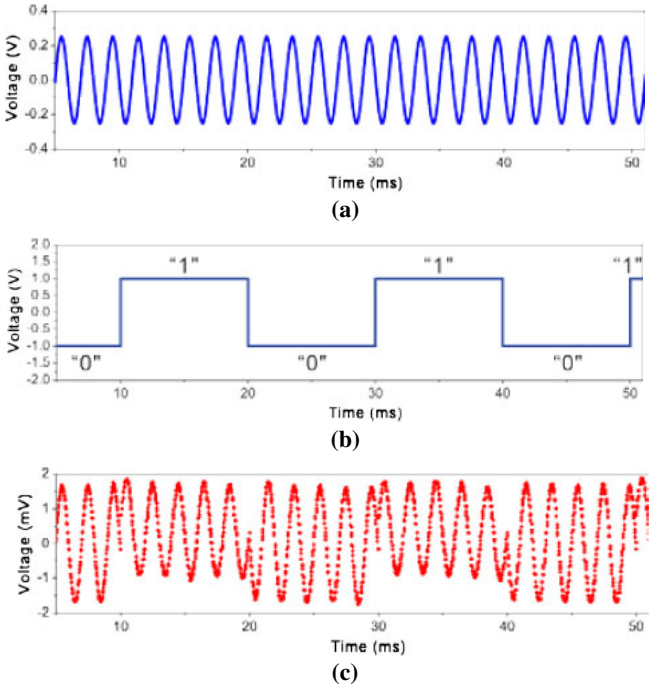


Fig. 5. (Color online) Operation of the graphene-based binary shift keying circuit. (a) Carrier signal with a frequency $f_{carrier} = 500\,Hz$. (b) Data input signal with a frequency $f_{data} = 50\,Hz$. (c) Output signal showing a clear 180° phase shift each time the data input signal changes for "0" and "1".

relation due to the relatively high source access resistance. Besides, scaling the gate length, the frequency performance of the devices can be improved by using thinner and higher quality gate dielectrics.

Demonstration of CVD Graphene devices operating up to 6.5 GHz is important for future flexible electronics and communication circuits. One of these applications is radio frequency identification (RFID) tags which utilize binary phase shift keying (BPSK) for coding and decoding information. Low cost and large area RFID tags are an area that could benefit greatly from large area CVD graphene.

4. Binary Phase Shift Keying

In this section, the graphene transistors described in §3 are used to demonstrate a BPSK circuit for modulating digital signals onto an analog carrier signal. Figure 4 shows the demonstration circuit. For this application, a digital square wave (data signal) and a high frequency sinusoid (carrier wave) are simultaneously applied to the gate of a graphene transistor, which is biased at the minimum conduction point by a DC source. The digital signal switches the channel of the GFET between electron and hole conduction. Due to the negative gain on the hole branch and the positive gain on the electron branch of the device transfer characteristics, the output signal is then equal to the carrier wave modulated by the data signal with 180° phase shift between "1" and "0" (Fig. 4).

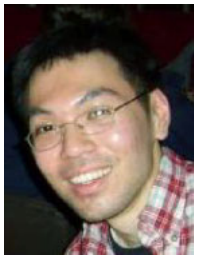
To demonstrate this experimentally, a carrier signal with $f_{carrier} = 500\,Hz$ [Fig. 5(a)] and a digital data signal $f_{data} = 50\,Hz$ [Fig. 5(b)] are supplied to the gate of the graphene transistor, which is biased to the minimum conduction point. The output signal measured by an Agilent 54642A oscilloscope is shown in Fig. 5(c). The 180° phase shift is clearly visible. Although, this demonstration is done at low frequency, the operating frequency is only limited by the speed of the GFET. In addition, this application, as for all analog signal processing applications, does not require a bandgap in graphene.[2–5)]

In conclusion, we have demonstrated and studied high frequency graphene field effect transistors fabricated on Cu-CVD graphene. These devices have an intrinsic f_T up to 3.5 GHz and an f_{max} of 6.5 GHz, and the use of substrate bias improves f_T by 75%. Through further optimization of gate dielectric, contact resistance, and scaling, RF device performance on CVD graphene may surpass that of traditional silicon electronics. Graphene circuits have also been demonstrated showing potential application areas in data transmission for BPSK.

Acknowledgements

This work is partially supported by the MSD Focus Center, the ONR GATE MURI project and the MIT/Army Institute for Soldier Nanotechnology. The authors would like to thank Sreekar Bhaviripudi for his help on the copper-based graphene growth.

1) X. Du, I. Skachko, A. Barker, and E. Y. Andrei: Nat. Nanotechnol. **3** (2008) 491.
2) H. Wang, D. Nezich, J. Kong, and T. Palacios: IEEE Electron Device Lett. **30** (2009) 547.
3) F. Traversi, V. Russo, and R. Sordan: Appl. Phys. Lett. **94** (2009) 223312.
4) N. Harada, K. Yagi, S. Sato, and N. Yokoyama: Appl. Phys. Lett. **96** (2010) 012102.
5) T. Palacios, A. Hsu, and H. Wang: IEEE Commun. Mag. **48** [6] (2010) 122.
6) K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov: Science **306** (2004) 666.
7) C. Berger, Z. Song, X. Li, X. Wu, N. Brown, C. Naud, D. Mayou, T. Li, J. Hass, A. N. Marchenkov, E. H. Conrad, P. N. First, and W. A. de Heer: Science **26** (2006) 1191.
8) A. Reina, X. Jia, J. Ho, D. Nezich, H. Son, V. Bulovic, M. Dresselhaus, and J. Kong: Nano Lett. **9** (2009) 30.
9) X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. Banerjee, L. Colombo, and R. Ruoff: Science **324** (2009) 1312.
10) J. S. Moon, D. Curtis, M. Hu, D. Wong, C. McGuire, P. M. Campbell, G. Jernigan, J. L. Tedesco, B. VanMil, R. Myers-Ward, C. Eddy, Jr., and D. K. Gaskill: IEEE Electron Device Lett. **30** (2009) 650.
11) Y. M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, Y. Y. Chiu, A. Grill, and Ph. Avouris: Science **327** (2010) 662.
12) S. Bae, H. Kim, Y. Lee, X. Xu, J.-S. Park, Y. Zheng, J. Baladrishnan, T. Lei, H. R. Kim, Y. I. Song, Y.-J. Kim, K. S. Kim, B. Özyilmaz, J.-H. Ahn, B. H. Hong, and S. Iijima: Nat. Nanotechnol. **5** (2010) 574.
13) X. Li, C. Magnuson, A. Venugopal, J. An, J. Suk, B. Han, M. Borysiak, W. Cai, A. Velamakanni, Y. Zhu, L. Fu, E. Vogel, E. Voelkl, L. Colombo, and R. Ruoff: Nano Lett. **10** (2010) 4328.
14) G. Dambrine, A. Cappy, F. Heliodore, and E. Playez: IEEE Trans. Microwave Theory Tech. **36** (1988) 1151.
15) Y. Hasumi, N. Matsunaga, T. Oshima, and H. Kodera: IEEE Trans. Electron Devices **50** (2003) 2032.



Allen Hsu received his B.S.E. from Princeton University in 2006 and M.S. from Massachusetts Institute of Technology in 2008 working on mid-infrared quantum cascade lasers. His current research interests are applications and fabrication of high-speed graphene electronics and photodetectors.

Han Wang received his B.A. and M. Eng. degrees in electrical and information science, both with highest honors, from Cambridge University, England, in 2006 and 2007. He is currently pursuing his Ph. D. degree in electrical engineering and computer science at MIT. He worked on modeling and simulation of power electronic devices from 2006 to 2007 in Cambridge University. At MIT since 2008, he has been working on graphene-based electronics and GaN based devices. His current research interest focuses on the development of graphene-based transistors for millimeterwave applications and the search for novel graphene-based ambipolar devices for applications in nonlinear electronics. His work at MIT also includes GaN-based transistors for high frequency and high power applications.

Ki Kang Kim received his B.A. and Ph. D. in physics from Sungkyunkwan University, South Korea in 2004 and 2008 respectively. Currently he is a post-doc in the Nano-materials and Electronics Lab at MIT. His research interests include doping of carbon based systems and growth mechanisms in low dimensional material systems.

Jing Kong received the B.S. degree from Peking University, Beijing, China, in 1997 and the Ph. D. degree from Stanford University, Stanford, CA, in 2002, both in chemistry. In 2004, she joined Massachusetts Institute of Technology, Cambridge, MA, where she is currently an Associate Professor with the Department of Electrical Engineering and Computer Science. She has worked in the field of carbon nanotubes for more than ten years and has published numerous papers on this subject. She and her colleagues at Stanford were among the first to develop the chemical vapor deposition method for synthesizing individual single-walled carbon nanotubes, and they also initiated the research on carbon nanotube chemical sensors. The research activity in her current group involves controlled synthesis of carbon nanotubes and graphene, investigation of their electronic and optical properties, and integration with the CMOS circuits.

Tomas Palacios is an associate professor in the Department of Electrical Engineering and Computer Science at the Massachusetts Institute of Technology, where he leads the Advanced Semiconductor Materials and Devices Group. He received his Ph. D. in electrical engineering from the University of California, Santa Barbara, and a B. Sc. degree from the Polytechnical University of Madrid, Spain. His research focuses on the development of new electronic devices to advance the fields of information technology, biosensors, and energy conversion. He is especially interested in expanding the frequency performance of GaN transistors, and developing new devices and circuits with graphene. His work has been recognized with multiple awards including the 2009 NSF CAREER Award, the 2009 ONR Young Investigator Award, the 2008 DARPA Young Faculty Award, the 2006 UCSB Lancaster Award, the Young Researcher Award at the 6th International Conference on Nitride Semiconductors, the Best Student Paper Award at the 63rd IEEE Device Research Conference, and the European Prize Salva i Campillo. He has authored more than 100 contributions on advanced semiconductor devices in international journals and conferences (35 of them invited), three book chapters, and eight patents.