

Design of Single-Switch Inverters for Variable Resistance / Load Modulation Operation

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Abstract—Single-switch inverters such as the conventional class E inverter are often highly load sensitive, and maintain zero-voltage switching over only a narrow range of load resistances. This paper introduces a design methodology that enables rapid synthesis of class E and related single-switch inverters that maintain ZVS operation over a wide range of resistive loads. We treat the design of Class-E inverters for variable resistance operation and show how the proposed methodology relates to circuit transformations on traditional class E designs. We also illustrate the use of this transformation approach to realize Φ_2 inverters for variable-resistance operation. The proposed methodology is demonstrated and experimentally validated at 27.12 MHz in a class E and Φ_2 inverter designs that operate efficiently over 12:1 load resistance range for an 8:1 and 10:1 variation in output power respectively and a 25 W peak output power.

I. INTRODUCTION

For frequencies above about 10 MHz, single-switch inverters such as the Class E inverter are often preferred. Fig. 1 shows the topology of the conventional Class E inverter, with the addition of a parallel-tuned output filter network L_P-C_P to improve output waveform quality. In the traditional Class E inverter [1, 2, 3], the input inductor L_F acts as a choke, while the tuned load network (C_F, L_S, C_S, R) is selected to both deliver power to the load resistor R and shape the switch voltage v_{DS} to provide zero-voltage switching (ZVS) and zero dv/dt turn on of the switch. Operation in this way – under ZVS with a single ground-referenced switch – facilitates switching at very high frequencies.

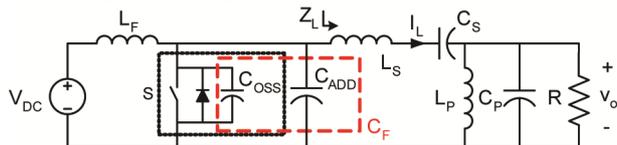


Fig. 1. Class E inverter topology, including parallel-tuned output filter. The capacitor C_F comprises the device output capacitance C_{oss} and additional capacitance C_{ADD} . It is also assumed that the switch has an antiparallel diode.

Because the load network is used to shape the switch voltage trajectory, the traditional Class E inverter is highly sensitive to variations in load resistance [2, 4],

and tends to deviate substantially from zero-voltage switching for load variations of more than about a factor of two or three in resistance. In many applications – such as when the load resistance is well known, or the inverter is coupled to the load via an isolator – this load sensitivity is not problematic. In other applications, however, it would be desirable to be able to operate efficiently over a wide range of resistive loads.

One application in which the effective load resistance can vary significantly is in dc-dc converters. In this case, the equivalent resistance provided by the rectifier can vary significantly with output voltage, instantaneous power, and input voltage [4-6]. While load variations in these applications can be compensated for with techniques such as resistance compression networks [4, 40, 41], these techniques increase component count and loss.

Another application in which the effective load resistance seen by the inverter varies over a wide range is in *outphasing* inverter systems. In outphasing, output power is controlled by phase-shifting the switching times of multiple inverters (i.e., phase-shift control of two or more inverters). When designed with an appropriate lossless power combiner – such as a Chireix combiner or multi-way lossless combiner – the real component of the effective load impedance seen by each inverter varies with control angle (thus controlling power), while the reactive component remains small [7-18, 33, 37, 38, 42-44]. For this reason, systems controlled in this manner are said to use *load modulation* to vary their output power. These systems must typically operate over a load resistance ratio that is equal or greater than the desired output power ratio obtained through load modulation. Direct load modulation of inverters can also be realized through electronic tuning of matching networks, as explored in [30, 31, 32].

While Class E and related inverters have been employed in applications with variable effective load resistance (e.g., [15, 16, 19, 30, 33]), a simple, complete and effective methodology for designing inverters for such conditions has been lacking. Prior to the authors' related conference publication on this topic [34] there has been some theoretical work on design of Class E inverters that are insensitive to load variations (e.g., [16, 20-22]). However, the results are complex, making design insight difficult, and some of these methods tend to lead to designs that have very high circulating

currents, which hurts efficiency. (With sufficiently high circulating currents, operation can be made insensitive to the load resistance, but the achievable practical efficiency of such designs is relatively poor.) Moreover, previous methods do not provide a means to effectively realize load modulation in single-switch inverter designs with higher-order tunings, such as those in [27, 28].

In this paper, we present a methodology for synthesizing single-switch resonant inverters for operation at fixed frequency with variable load resistance (i.e., with load modulation). The proposed approach can be applied to both class E inverters and to higher-order tuned converters such as the class Φ_2 inverter [27] and similar designs [28]. To provide greater flexibility of operation, we allow for waveforms that ideally maintain ZVS switching and constant switch duty ratio, but do not necessarily maintain zero dv/dt turn-on of the transistor as load resistance varies. We focus on identifying the resonant frequencies and characteristic impedances of the key resonant networks in the circuit, and provide guidance of how circuit performance is modified by adjusting these parameters.

In section II of the paper, we introduce an equation-based version of the design methodology as applied to the Class E inverter of Fig. 1. The methodology is demonstrated in Section III and experimentally validated in Section IV. Section V shows how this design methodology is developed based on circuit transformations on classical Class E designs [1-3], and provides a means to transform existing class-E inverter designs to a form more suitable for load modulation. Section VI shows that the circuit-transformation methodology can also be employed in single-switch inverters with higher-order tunings to obtain designs maintaining good performance under load modulation. This is done in the context of an example Φ_2 inverter design and experimental results are provided that demonstrate the efficacy of this technique. Lastly, Section VII concludes the paper. Appendix I provides a detailed theoretical discussion of the basis for selecting key inverter design parameters.

II. DESIGN METHODOLOGY

We start by outlining a frequency-tuning-based design method for load modulated class E inverters. This method enables class E designs for load modulation to be rapidly synthesized. The proposed design method was arrived at through the circuit transformation methodology we introduce in Section V, coupled with an extensive investigation of performance across a range of design options. Details behind the selection of particular design parameters are thoroughly discussed in Appendix I.

To design the class E inverter for load modulation, one starts with a set of output specifications: output frequency f_{sw} , rated output power P_{or} , and a load resistance range (from minimum rated load resistance R_{min} to a maximum load resistance R_{max}). Output power P_o , load resistance R , and dc input voltage V_{DC} are approximately related as follows:

$$\frac{P_o R}{V_{DC}^2} = 1.32 \quad (1)$$

The product of power, resistance and the inverse square of voltage being held constant in design is typical in single switch converters (e.g., see [2,3]). Power being proportional to the square of dc voltage owes to the fact that this is a switched linear system with all power delivered to the output, and power being inversely proportional to resistance owes to the fact that the resistor voltage (ideally) does not change with resistance. The proportionality constant was found through numerous simulations and well represents systems designed with the proposed approach; its value is close to but slightly larger than that found theoretically by assuming that the switch voltage is a half-sine wave and the output filter perfectly extracts the fundamental component. The rms output voltage amplitude, $V_{o,rms}$, is approximately 1.15 times the dc input voltage, and is approximately invariant to load resistance, so R_{min} sets the rated output power and R_{max} sets the minimum output power.

For the design procedure, it is assumed that transistors of appropriate characteristics (on-state resistance, voltage and current ratings, and capacitances) can be obtained. The design goals are to select input network component parameters L_F and C_F , and output network component parameters (L_S , C_S , L_P and C_P). It is assumed that the total capacitance C_F includes transistor output capacitance C_{oss} . Moreover, we assume that all components are linear (neglecting variations of C_{oss} with voltage on circuit operation, as treated in [23-26].) It is also assumed that the transistor is operated at 50% duty ratio.

A key observation we have made is that to achieve good performance under load modulation, the load network impedance Z_L should remain substantially resistive as load resistance R varies. This condition ensures that the fundamental component of the load current I_L (see Fig. 1) is in phase with the fundamental component of the drain voltage. As Appendix I demonstrates in detail, this is a necessary condition for maintaining ZVS across load modulation. Consequently, we tune both the L_S , C_S network and the L_P , C_P network to be resonant at the switching frequency:

$$\frac{1}{\sqrt{L_P C_P}} = \frac{1}{\sqrt{L_S C_S}} = 2\pi f_{sw} \quad (2)$$

Note that this design selection is different than those proposed previously for operation under varying load [16, 19-21].

The characteristic impedances of the L_S , C_S and L_P , C_P networks are selected such that adequate filtering of the output voltage is achieved across the intended load modulation range. While this selection is highly application dependent, one possible selection method is to choose the parallel network to provide high filtering for the lightest load (largest resistance), and the series network to provide high filtering at the heaviest load (smallest / rated resistance), and to rely on a combination

of series and parallel filtering in the mid range (e.g., near the geometric mean of minimum and maximum resistances). Thus, one might choose:

$$\frac{\sqrt{L_S/C_S}}{R_{\min}} = \frac{R_{\max}}{\sqrt{L_P/C_P}} = Q_{fil} \quad (3)$$

with Q_{fil} selected in the range of 2 to 10 for adequate filtering over a 10:1 load resistance range. Note that although larger values for Q_{fil} result in output voltage waveforms with less harmonic content, they also give rise to higher circulating currents in the output tank, and hence yield higher resonating power losses. On the other hand, lower Q_{fil} values lead to higher harmonic content in the output, but result in less power losses due to circulating currents in the output tank. It can be shown that the ability of the inverter to maintain ZVS across load modulation improves with reducing the harmonic content of its output load current. In any case, however, selecting Q_{fil} much larger than 10 may be impractical and hard to realize, especially at higher RF frequencies. On the other hand, extensive circuit simulation indicates that a Q_{fil} of less than 2 gives rise to appreciable harmonic content in the output, which in turn results in reducing the load modulation range over which the inverter can be designed to maintain ZVS.

It should be noted that other filter structures may be selected, but should be chosen with the goal that the input impedance of the load network (Z_L in Fig. 1) remain resistive at the switching frequency as the load resistance changes. Likewise, to provide impedance transformation between the inverter and the load, one should utilize a method that maintains resistive input impedance of the load at f_{SW} as the load varies, such as a tuned transformer, an immittance conversion network, or a quarter-wave line [45].

The characteristic impedance of the L_F, C_F network is selected based on the rated (minimum) load resistance:

$$\sqrt{L_F/C_F} = k_f R_{\min} \quad (4)$$

where k_f is a design value typically selected between 0.2 and 1.5. As will be shortly described and discussed in detail in Appendix I, this range of k_f values is a result of the tradeoff between resonating losses and the load modulation range over which the inverter can maintain ZVS. To the extent that soft switching can be maintained, higher values of k_f are preferable because they increase characteristic impedance and reduce the resonating losses associated with the L_F, C_F network, which do not reduce significantly as load resistance increases (and operating power reduces). However, lower values of k_f yield higher values of C_F , and hence higher allowable values of transistor output capacitance, which forms part or all of C_F . Lower values of k_f also reduce L_F , enabling faster dynamic response of the inverter to changes in operating condition. In practice, one starts with a low value of k_f , and increases it as much as possible within the constraints of maintaining ZVS (or close to it) across the load range, providing at least the

minimum amount of capacitance associated with the transistor, and achieving the needed response speed.

To achieve the desired soft-switching performance across load modulation, the input-side network L_F, C_F must be tuned to resonance at an appropriate frequency depending on the characteristic impedance of the input tank and the load modulation range. As Appendix I demonstrates, there is no single resonant frequency f_{IN} of L_F and C_F that will guarantee perfect ZVS across the entire load modulation range. In other words, for a given input tank characteristic impedance Z_{IN} , the appropriate f_{IN} to ensure ideal ZVS varies with load. It can be shown (see Appendix I) that as the inverter's minimum load resistance decreases compared to Z_{IN} , the correct f_{IN} for ZVS will approach 1.29 times the switching frequency f_{SW} . Appendix I further demonstrates that the variation of f_{IN} (necessary for ZVS) with load variation decreases with decreasing Z_{IN} compared to the inverter's rated (minimum) load resistance, i.e. with decreasing k_f values in (4). For example, for a 10:1 load variation and $k_f = 1.25$, the necessary f_{IN} for ideal ZVS varies between 1.29x and 1.5x the switching frequency. On the other hand, for $k_f = 0.2$ and the same load modulation range, the necessary f_{IN} for ZVS is nearly invariant and approximately equal to 1.29x the switching frequency.

In reality however, the input tank must be tuned to resonate at only one particular frequency, and one does not have the luxury to change f_{IN} with load variation. Thus f_{IN} must be selected to provide near-ZVS across load modulation, and it is typically chosen to be 1.3 to 1.5 times the switching frequency:

$$1/\sqrt{L_F C_F} = 2\pi f_{IN} \quad (5)$$

This aspect of the tuning is in a similar range as that selected for the designs in [16, 35], which tune the input network at 1.3 and 1.41 times the switching frequency respectively, though other aspects are different. Usually, one would tune the input tank to resonance at a frequency f_{IN} that ensures the inverter is truly zero-voltage switching at rated or near rated load. As shown in Appendix I, as the output power is backed-off (load resistance is increased), the f_{IN} necessary for ideal ZVS decreases. Since however the input tank is already tuned at a frequency which ensures ZVS at rated load, increasing its load resistance will cause a negative turn-on voltage across the switch. In the case of implementing the switch with a FET, this negative turn-on voltage will be clamped by the forward-voltage drop of the body diode. As a result, the inverter will continue to maintain near-ZVS with further increase of load resistance. It is noted that in some devices having a body diode, there may be additional reverse recovery losses if the body diode conducts. The GaN HEMT devices used in the present work do not have body diodes per se; rather, reverse conduction is through the device channel, so such reverse recovery loss is not of concern. Appendix I provides additional details on the selection of f_{IN} for a particular load modulation range and input tank characteristic impedance. We have found that the above methodology, used in conjunction with a circuit simulator such as SPICE, allows rapid design of

inverters that operate well over a wide range of load resistances.

III. EXAMPLE AND DEMONSTRATION

This section illustrates how the proposed class E design methodology can be applied, and presents simulation results that demonstrate its efficacy. (Experimental results are presented in the following section.) The design procedure begins with a rated load resistance, rated output power and switching frequency. Table I summarizes parameters chosen for the example we carry out here.

TABLE I. DESIGN PROCEDURE EXAMPLE INPUT DATA.

Parameter		Value
Rated load resistance	$R_{or} = R_{min}$	12.5 Ω
Rated output power	P_{or}	25 W
Switching frequency	f_{sw}	27.12 MHz

Based on these values, we can calculate the rms value of output voltage V_{or} (6), rated output rms current I_{or} (7) and DC supply voltage V_{DC} (8).

$$V_{or} = \sqrt{P_{or} R_{or}} = \sqrt{25 \text{ W} \cdot 12.5 \Omega} = 17.68 \text{ V} \quad (6)$$

$$I_{or} = \sqrt{\frac{P_{or}}{R_{or}}} = 1.41 \text{ A} \quad (7)$$

$$V_{DC} = \frac{V_{or}}{1.15} = 15.37 \text{ V} \quad (8)$$

The next step is to choose the parameters L_S and C_S . As per (2), these are chosen to resonate at the switching frequency. In addition, we select a Q factor of the circuit at rated load as per (3). Here we select $Q_{fil} = Q_s = 5$:

$$\frac{\sqrt{L_S/C_S}}{R_{min}} = 5 \quad (9)$$

This leads to the following results:

$$C_S = \frac{1}{2\pi f_1 Q_s R_{or}} = 93.9 \text{ pF} \quad (10)$$

$$L_S = Q_s^2 R_{or}^2 C_S = 367 \text{ nH}. \quad (11)$$

A similar approach is applied to design the parallel resonant output filter. In this example, its quality factor is chosen to $Q_{fil} = Q_p = 4.5$ when the load resistance is ten times higher than the rated resistance (the highest considered resistance):

$$\frac{R_{max}}{\sqrt{L_P/C_P}} = \frac{10 \cdot R_{or}}{\sqrt{L_P/C_P}} = 4.5 \quad (12)$$

This leads to results:

$$L_P = \frac{10 R_{or}}{2\pi f_1 Q_p} = 147 \text{ nH} \quad (13)$$

$$C_P = \frac{Q_p^2 L_P}{R_{or}^2} = 293 \text{ pF}. \quad (14)$$

Calculation of the L_F - C_F resonant circuit parameters begins with the determination of the input tank characteristic impedance. For the present design, we select $k_f = 0.7$. According to (4) we then have:

$$Z_{charF} = 0.7 R_{or} = 8.75 \Omega \quad (16)$$

Next, we determine the resonant frequency f_{IN} of the input network L_F - C_F . SPICE simulations of the circuit model indicate that in order to maintain soft-switching, f_{IN} in (5) must be selected to be approximately 1.5 times the switching frequency:

$$f_{IN} = 1.5 \cdot f_{sw} = 40.68 \text{ MHz}. \quad (15)$$

L_F - C_F are determined from circuit resonant frequency and characteristic impedance as follows:

$$C_F = \frac{1}{2\pi f_f Z_{charF}} = 447 \text{ pF} \quad (17)$$

$$L_F = C_F Z_{charF}^2 = 34.2 \text{ nH}. \quad (18)$$

For the given parameters, the EPC 1007 transistor has been chosen. Its capacitance is simply approximated as a linear capacitance $C_{oss} = 100 \text{ pF}$. To provide the desired operation, we augment C_{oss} with an additional capacitance C_{ADD} :

$$C_{ADD} = C_F - C_{oss} = 337 \text{ pF} \quad (19)$$

Calculated parameters are then slightly adjusted using simulation. The nominal circuit parameters for the design (including both from the initial design pass and with adjustments based on simulation) are shown in Table II.

TABLE II. COMPONENT AND PARAMETER VALUES FOR DESIGNED CLASS E INVERTER.

Component	Values from design procedure	Adjusted values after SPICE simulation
L_F	34.2 nH	34.2 nH
C_F	447 pF	516 pF
C_{ADD}	347 pF	366 pF
L_S	367 nH	367 nH
C_S	93.9 pF	93.9 pF
L_P	147 nH	147 nH
C_P	293 pF	293 pF
v_{DC}	15.37 V	16 V
f_{sw}	27.12 MHz	27.12 MHz
D	50%	50%

Fig. 2 shows simulated drain-source voltage waveforms for an inverter based on our proposed design methodology, while Fig. 3 shows results from a conventional class-E design (a design at $Q=10$ based on [3]). The simulations utilize a simple switch model with an on-resistance $R_{ds} = 0.3$ and a linear output capacitance

$C_{oss} = 100$ pF for the switch. Components used in the proposed design are presented in Table II, while components for the conventional design are presented in Table III.

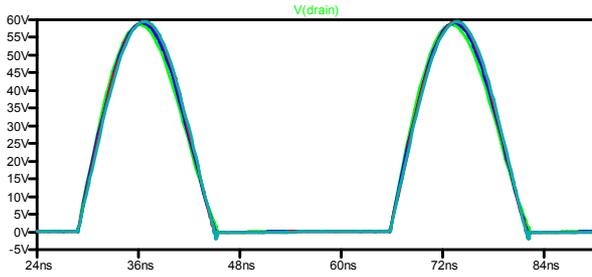


Fig. 2. v_{DS} waveforms of the proposed Class E inverter of Table III (for 1, 2, 5 and 10 times rated resistance of 12.5Ω).

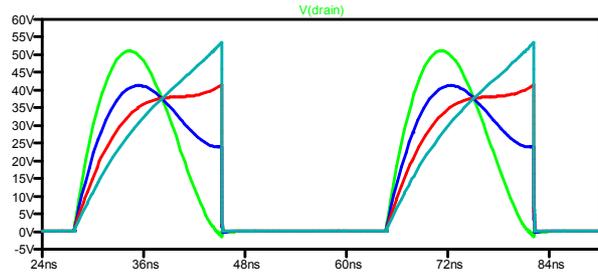


Fig. 3. v_{DS} waveforms of the classical Class E inverter ($Q=10$ Design, [3], components in Table III) (for 1, 2, 5 and 10 times rated resistance).

TABLE. III. COMPONENT VALUES FOR CLASSICAL CLASS E INVERTER.

Component	Values from Spice simulation
L_F	100 μ H
C_F	199 pF
C_{ADD}	99 pF
L_S	734 nH
C_S	47 pF
L_P	-
C_P	-
v_{DC}	16 V
f_{SW}	27.12 MHz
D	50%
$R_{or}=R_{min}$	12.5 Ω

It can be seen that a class-E inverter based on the methodology proposed here achieves much better switching waveforms across load resistance (i.e., at or near ZVS) than a traditional class E design though it does not provide zero dv/dt turn-on of the switch. It is noted that the voltage stress of the converter designed for load modulation is slightly higher than that for a conventional class E inverter ($\sim 10\%$); this may represent a slight disadvantage in some design cases, especially if operation over a wide range of load resistances is not of interest.

IV. EXPERIMENTAL RESULTS

To further validate the proposed approach, an experimental prototype has been developed and evaluated. Fig. 4 shows the prototype, which approximately realizes the example design of the last section (components listed in Table IV.) In addition to using paralleled off-the-shelf inductors to construct L_F , a version of the converter with a custom single-turn foil inductor having a higher Q was also tested. The gate

driver comprised a parallel connection of six inverters (three NC7WZ04 integrated circuits). The inverters were controlled by a function generator. The gate driver circuit supply power never exceeded 100 mW. The inverter was constructed on a four layer PCB with 2 oz outer and 1 oz inner copper layers. The load for the inverter comprised paralleled resistors soldered directly to the PCB. The load resistors were cooled through the PCB by mounting the back of that portion of the PCB to a Dynatron P199 CPU cooler.

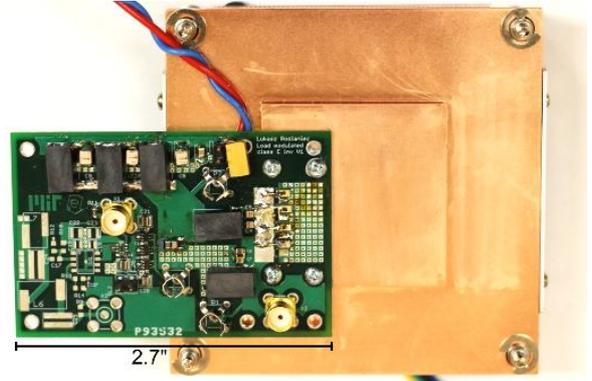


Fig. 4. Photograph of the prototype inverter with resistive load and load heat sink. This version of the inverter utilizes three parallel inductors to form L_F (Maxi-Spring 132-09, Coilcraft Inc.). The design was also tested with a large single-turn foil inductor that provided higher Q .

TABLE. IV. COMPONENT VALUES FOR THE PROTOTYPE CLASS E INVERTER.

Component	Value	Implementation
L_F	35.6 nH	3 parallel maxi-spring inductors (132-09, Coilcraft Inc.)
C_{ADD}	377 pF	ATC 700A
L_S	380 nH	maxi-spring 132-17, Coilcraft Inc.
C_S	90 pF	ATC 700A
L_P	169 nH	maxi-spring 132-12, Coilcraft Inc.
C_P	203 pF	ATC 700A
R_{o-r}	12.5 Ω	4 parallel Bourns CHF1206CNT500LW resistors
R_{max}	150 Ω	Series connection of Bourns CHF2010CNP101RX and CHF1206CNT500LW resistors
Switch	$C_{oss} \sim 100$ pF $R_{on} \sim 0.03 \Omega$	EPC 2007
v_{DC}	16 V	-
f_{SW}	27.12 MHz	-
D	50%	-

Fig. 5 shows the experimental test setup. The prototype class E circuit validates the proposed design approach. Input power measurements were based on dc input current and voltage measurements using multimeters. Output power was measured by means of oscilloscope-based rms voltage measurements and knowledge of the load resistance (and thus includes the modest harmonic contributions to output power). Efficiency results across load are shown in Fig. 6. Experimental waveforms at rated load resistance and 12X rated load resistance are shown in Fig. 7 and Fig. 8 respectively.

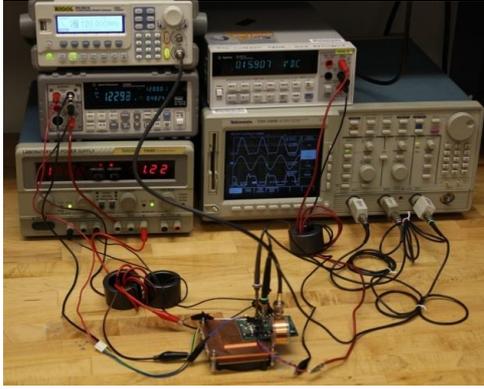


Fig. 5. Photograph of the experimental setup. This version of the circuit incorporates the custom foil inductor.

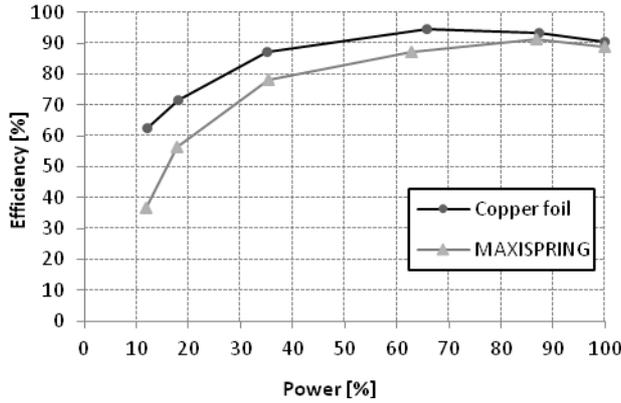


Fig. 6. Inverter drain efficiency as a function of output power (adjusted by resistive load modulation). The efficiency is found at the following load resistances: $R = 12.53 \Omega$, 16.47Ω , 24.61Ω , 49.3Ω , 99.3Ω and 149.1Ω . Efficiency is shown for both the baseline design (with L_F formed from paralleled Maxi-spring inductors) and with a custom foil inductor for L_F .

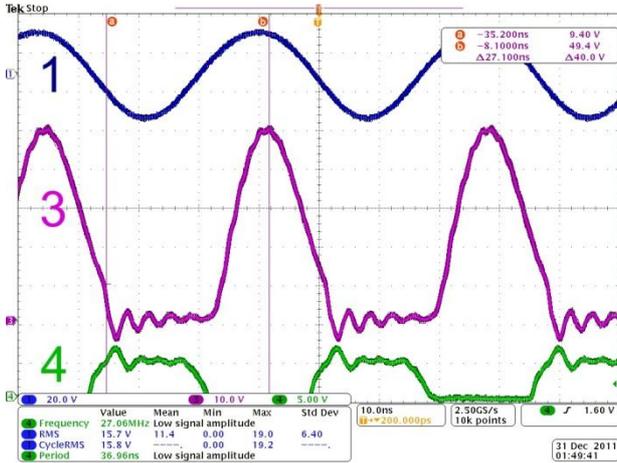


Fig. 7. Waveforms of the prototype class E inverter at rated load ($R_o = 12.53 \Omega$) ($1 - v_o$, $3 - v_{ds}$, $4 - v_g$).

It can be seen that near-zero-voltage switching is maintained over the 12:1 load resistance range. Unlike the simulation, however, the experimental inverter begins to lose soft switching at one end of the operating range. (It is believed that this results partly from the nonlinearity of the device capacitance, which was not modeled in the simulation.) A 12:1 variation in load resistance results in an 8.3:1 variation of output power. This indicates that the system provides an rms output voltage that is nearly (but not perfectly) invariant to the value of load resistance. Fig. 6 shows efficiency vs. output power, with power

varied by adjusting the load resistance. It can be seen that efficiency remains high over a very wide power (and load resistance) range. At very low output power levels, losses due to circulating currents in the L_F - C_F input network become increasingly important and degrade system efficiency. (This underscores the benefit of using a high-Q inductor for the input resonant inductor L_F , and in keeping the characteristic impedance of the input-side tank as high as possible considering soft-switching requirements.)

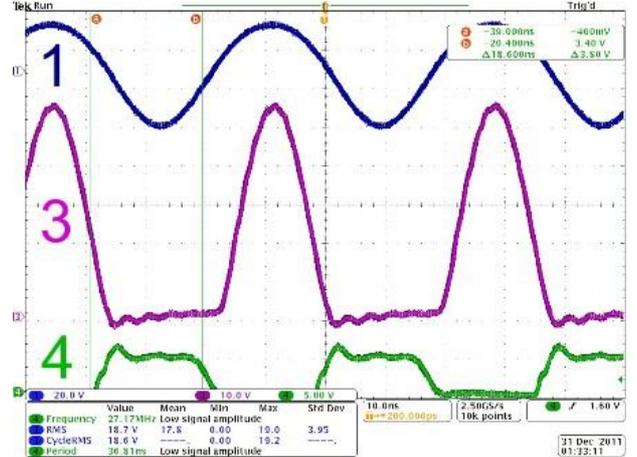


Fig. 8. Waveforms at 12 times rated load resistance and 12% of rated load power ($R_o = 149.1 \Omega$) ($1 - v_o$, $3 - v_{ds}$, $4 - v_g$).

V. CIRCUIT TRANSFORMATION VIEW

In this section, we show how circuit transformations can be applied to existing inverter designs (such as the conventional class E inverters of [2,3]) to realize inverters having similar circuit values and properties to those developed with the methodology of Section II. The circuit transformation technique we introduce can be used to retune existing designs to better accommodate load resistance variation, and combined with other design techniques (e.g., [25]) to better account for factors such as device capacitance nonlinearity.

Consider the transformation steps in Fig. 9 (a)-(d). The circuit of Fig. 9(a) can represent a conventional class E design, such as a design from [3] with a high loaded Q and a large-valued dc choke inductor L_{DC} . In such a design, the resonant network impedance Z_L is inductive at the switching frequency. Consequently, as shown in Fig 10(b), one can split the LC tank into two portions – a series resonant network L_T , C_T tuned to the switching frequency and an additional inductor L_{NET} . If the output tank is of sufficiently high quality factor, it carries a nearly sinusoidal current at the switching frequency. In this case, as illustrated in Fig. 9(c), series-connected components L_{NET} and R can be replaced with a parallel network (L_K and R_K) having the same impedance at the switching frequency. The values of the transformed components may be found as [28]:

$$L_K = L_{NET} \left(1 + \frac{1}{Q_T^2} \right) \quad (20)$$

and

$$R_K = R \left(1 + Q_T^2 \right) \quad (21)$$

where

$$Q_T = \omega L_{NET} / R \quad (22)$$

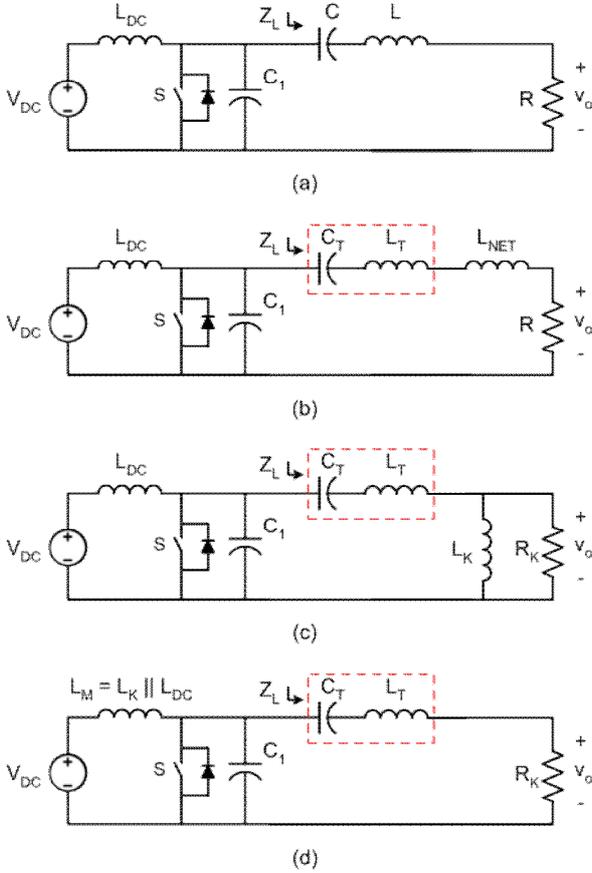


Fig. 9. Steps for transforming a class E resonant inverter for variable-resistance operation.

Considering the network of Fig. 9(c), the tank network $L_T C_T$ is a short circuit (due to resonance) at the switching frequency. At this frequency (only), inductor L_K is effectively in parallel with the input choke inductor L_{DC} (from an ac perspective). As our last transformation step, illustrated in Fig. 9(d), we thus eliminate L_K , and replace L_{DC} with a new inductor L_M having a value of $L_K \parallel L_{DC}$.

The result of the transformation illustrated in Fig. 9 yields a circuit in Fig. 9(d) that has the output network tuned on resonance at the switching frequency, which we have found to be a desirable characteristic to achieve good operation over a wide load resistance range. Moreover, the input inductor in the transformed circuit is a resonant inductor rather than a simple dc choke. The behavior of the circuit of Fig. 9(d) will not necessarily be the same as that of Fig. 9(a), since two of the transformation steps employed preserve impedance characteristics only at the switching frequency, but not at dc or harmonic frequencies. Nonetheless, this transformation yields designs that are quite close to those produced by the methodology of Section II, and which maintain desirable operation over a wide load resistance range.

As an example of this transformation approach, we start with a conventional class E inverter design from [3] with $Q = 100$ and a 50% switch duty ratio. From [3], the components for the circuit of Fig. 9(b) are defined by:

$$\omega R C_1 = 0.1851; \quad (22)$$

$$\omega R C_T = 0.01006; \quad (23)$$

$$\omega L_T / R = 99.4036; \quad (24)$$

and

$$\omega L_{NET} / R = 1.1764 \quad (25)$$

Transforming to the circuit of Fig. 9(c), we get

$$R_K = 2.3839 \cdot R \quad (26)$$

and

$$\omega L_K = 2.027 \cdot \omega L_{NET} = 2.3846 \cdot R \quad (27)$$

Finally the circuit of Fig. 9(d) results in the same values for C_1 , C_T , L_T and R_K , with

$$\omega L_M = 2.027 \cdot \omega L_{NET} = 2.3846 \cdot R. \quad (28)$$

Examining this design, we find that:

$$\frac{1}{\sqrt{L_M C_1}} = 1.5052 \omega \quad (29)$$

such that the input network is tuned almost exactly to 1.5 times the switching frequency, and the output network is tuned to the switching frequency, just as in the design methodology of Section II. With addition of a tuned parallel resonant tank in parallel with the load resistor for filtering (and with appropriate renaming of components) we obtain a design very close to that provided by the direct design method of Section II.

The transformation technique of Fig. 9 is thus useful for converting existing class E inverter designs into alternative designs that are suitable for load modulation. Moreover, this transformation provides an approximate way to relate conventional class E designs to those generated by the methodology developed in Section II. Furthermore, in the following subsection, we demonstrate how this approach can be effectively applied to Φ_2 inverter designs [27] and designs similarly employing higher order tunings (e.g., [28]) to yield inverters suitable for load modulation operation.

VI. CIRCUIT TRANSFORMATION OF A Φ_2 INVERTER

In a traditional class E inverter, the peak switch voltage stress is ideally about 3.6 times the input voltage [1], [2]. However, the non-linear characteristic of the device capacitance with drain voltage may further increase the voltage stress to more than 4 times the input voltage [23]. In contrast, by employing higher-order tunings, reduced device stress is achievable. For example, using a tuned resonant input network, a Φ_2 inverter achieves zero-voltage switching and low device voltage stress [27]. An important feature of the Φ_2 converter of Fig. 10 is the $L_{MR} - C_{MR}$ series branch which is tuned to be resonant near the second harmonic of the switching frequency, thus suppressing second harmonic content in

the drain voltage and providing a quasi-trapezoidal drain voltage waveform. F_2 inverters are useful in very high-frequency dc-dc converters, for example [39, 46-49].

Fig. 10 shows a schematic of a Φ_2 inverter driving a load R_L and having an input voltage V_{DC} . The switch is realized with a MOSFET having a drain-to-source capacitance C_{OSS} .

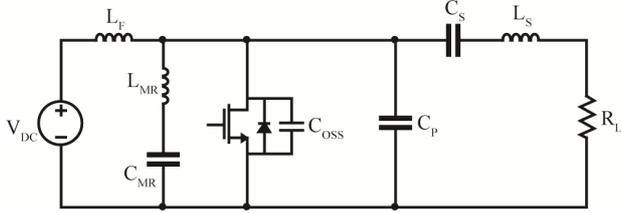


Fig. 10. Schematic of the Φ_2 inverter with an input voltage V_{DC} and a load R_L .

By carefully tuning the components of the inverter, the peak voltage across the switch can be minimized while maintaining switched-mode operation with near zero-voltage turn-on and turn-off at given frequency and duty ratio [27]. As this inverter is usually designed using frequency-domain tuning techniques [27, 39], and there are an infinite number of possible implementations, transformation-based methods are highly useful in realizing designs for load modulation operation.

The ringing characteristic of the drain-to-source voltage during the period when the switch is in the "off" state is determined by the impedance Z_{ds} seen looking into the circuit port defined by the drain. By appropriately tuning the inverter components so that Z_{ds} is high at the fundamental and third harmonics and low at the second harmonic, a quasi-trapezoidal drain-to-source voltage waveform can be obtained. Furthermore, as [27] demonstrates, in order to obtain such a drain-to-source voltage waveform, the impedance Z_{ds} at the fundamental of the switching frequency must be 30° to 60° inductive.

A detailed methodology for the design of the Φ_2 inverter and for selection of its components is provided in [27]. According to this methodology, the Φ_2 inverter is designed for a particular load R_L . The values of C_S and L_S are selected to achieve the desired power transfer based on the voltage division from the trapezoidal drain voltage waveform resulting from the impedances of C_S , L_S and R_L . As a result of this design methodology, load modulation of the inverter could significantly alter its drain impedance Z_{ds} (especially its phase). Consequently this may distort the desired trapezoidal drain voltage waveform causing loss of zero-voltage switching and inevitable reduction of the overall inverter efficiency. Using a transformation-based approach, one can synthesize an alternative Φ_2 design that does not have the same constraints.

To illustrate the transformation approach in the context of the Φ_2 inverter, consider a traditional Φ_2 inverter designed according to the methodology outlined in [27] with $L_F = 110$ nH, $L_{MR} = 90$ nH, $C_{MR} = 95.7$ pF, $C_P = 100$ pF, $C_S = 96.5$ pF, $L_S = 430$ nH. The inverter is designed to operate at 27.12 MHz and deliver up to 25 W to a 12.5 Ω resistive load for an input voltage V_{DC} of 30 V. The semiconductor switch is implemented with a 100 V GaN MOSFET (EPC2007, EPC) with an on-resistance $R_{ds,ON}$ of approximately 30 m Ω , and an intrinsic output capacitance C_{OSS} of 118 pF at a drain-to-source voltage $V_{DS} = 50$ V.

The switch is operated with 30 % duty-cycle. Similarly to the class E inverter design described above, the gate driver comprises a parallel combination of six inverters (NC7WZ04, Fairchild Semiconductor). The inverters are operated with a supply voltage of 3.8V and are driven by a 27.12 MHz sine wave with amplitude of 4.2 V_{pp} and a DC offset of 3.22 V (generated by a function generator). Fig. 11 shows the Φ_2 inverter board, while Table V lists the components used in its implementation and describes their respective realization.



Fig. 11. Photograph of the traditional Φ_2 inverter designed according to [27] (see Fig. 13a). PCB size is 42 mm x 57mm. The transformed version of the Φ_2 inverter (Fig. 13d) has an identical PCB layout, although it is populated with different components.

Fig. 12 depicts the measured drain voltage waveforms for the above Φ_2 inverter design with $V_{DC} = 30$ V for 1x, 2x, 4x, and 10x its rated load resistance $R_L = 12.5$ Ω (the minimum load resistance for which the inverter is designed). As can be seen, when the inverter is loaded with its rated load R_L its drain voltage is quasi-trapezoidal with a peak switch voltage stress of about twice the input voltage. Under this loading condition, the MOSFET clearly exhibits zero-voltage turn-on. However as the inverter loading resistance is increased, it can be seen that the trapezoidal shape of the switch drain voltage is significantly altered, and zero-voltage switching is lost.

TABLE. V. COMPONENT VALUES FOR THE TRADITIONAL Φ_2 INVERTER OF FIG. 13A.

Component	Value	Implementation
L_F	110 nH	Coilcraft Inc. 2222SQ-111GEB
L_{MR}	90 nH	Coilcraft Inc. 2222SQ-90NGEB
C_{MR}	95.7 pF	ATC 100B 2R7BW in parallel with ATC 100B ATC 100B 820JW
L_S	430 nH	Coilcraft Inc. 2929SQ-431GEB
C_S	96.5 pF	ATC 100B 8R2CW in parallel with ATC 100B 820JW
C_P	100 pF	ATC 100A 820JW
Switch	$C_{OSS} \sim 118$ pF $R_{ds,ON} \sim 30$ m Ω	EPC 2007

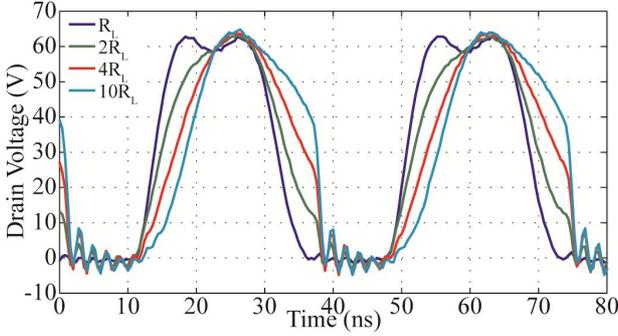


Fig. 12. Drain voltage of the Φ_2 inverter of Fig. 10 with $L_F = 110$ nH, $L_{MR} = 90$ nH, $C_{MR} = 95.7$ pF, $C_p = 100$ pF, $C_s = 96.5$ pF, $L_s = 430$ nH, and $V_{DC} = 30$ V for various resistive loads. The rated (minimum) load resistance is $R_L = 12.5$ Ω .

Let us now apply the circuit transformations discussed in Section V to the Φ_2 inverter design considered above and examine the effect of load modulation on its drain voltage waveform. Fig. 13 illustrates the steps for transforming the Φ_2 inverter for variable load resistance operation. The 430 nH output inductor (L_s) of the original inverter design can be thought of as a series combination of 357 nH and a 73 nH inductors (see Fig. 13a). Note that the 357 nH is in resonance with the 96.5 pF capacitor at the 27.12 MHz switching frequency.

As a next step (see Fig. 13b), the series combination of the 73 nH and the 12.5 Ω load ($Q = 1.00$ at 27.12 MHz) can be converted to their parallel circuit equivalent as per (20)-(22). This series-to-parallel transformation is only valid at the inverter's switching frequency. Since at 27.12 MHz the 96.5 pF capacitor and 357 nH inductor are in resonance, the 146 nH load inductor (Fig. 13b) is effectively connected in parallel with the 110 nH input inductor. In turn, the parallel combination of the 146 nH and 110 nH inductors can be equivalently replaced by a 62.7 nH inductor (Fig. 13d). Note that the circuit transformation from Fig. 13b to Fig. 13c is strictly valid only at the inverter's switching frequency. It can be shown however that the non-validity of this transformation at higher harmonics of the switching frequency has only a minor impact on the inverter's performance. This is especially true for inverter designs with low harmonic content in their output. The above circuit transformation does have a minor effect on the drain impedance Z_{ds} at higher harmonics of the switching frequency. Nevertheless, at the inverter's 27.12 MHz switching frequency, the phase and magnitude of the drain impedance remain unchanged; it is this impedance phase and magnitude that are of greatest significance to the shaping of the drain voltage waveform [27]. For sake of clarity, let us refer to the inverters of Fig. 13a and Fig. 13d as the traditional and transformed inverter designs respectively.

Note that although the traditional inverter (Fig. 13a) is designed for a 12.5 Ω load, after applying the circuit transformations, the nominal load of the transformed inverter for rated power is 25 Ω . Of course, if one still desires to employ the modified design in the original application, namely to drive a nominal 12.5 Ω load, an additional impedance transformation stage may be included.

The PCB layout of the transformed Φ_2 inverter is identical to that of the traditional inverter (see Fig. 11). The components used in the implementation of the transformed inverter are listed in Table VI.

Note that due to availability of component values, the 62.7 nH input inductor in Fig. 13d is implemented as a 68 nH inductor. As a consequence, the 100 pF C_p capacitor is slightly reduced to 80 pF to preserve ZVS. For similar reason, the 357 nH output inductor L_s (see Fig. 13d) is implemented as a 360 nH inductor, and consequently, C_s is slightly reduced to 95.7 pF to maintain resonance of C_s and L_s at the inverter's switching frequency.

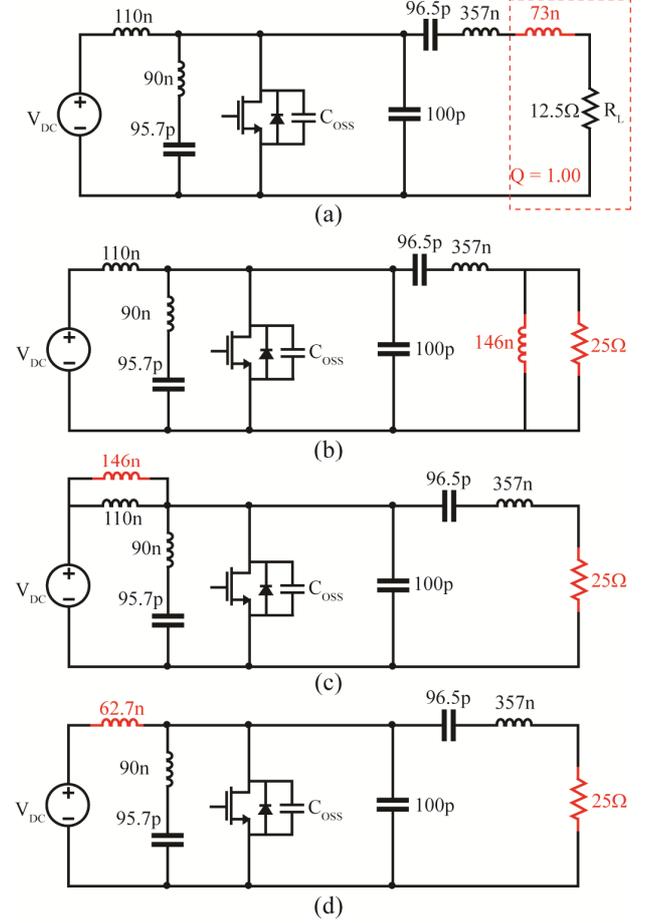


Fig. 13. Steps for transforming a class Φ_2 inverter for variable-load operation.

TABLE VI. COMPONENT VALUES FOR THE TRANSFORMED Φ_2 INVERTER OF FIG. 13D.

Component	Value	Implementation
L_F	68 nH	Coilcraft Inc. 1515SQ-68NGEB
L_{MR}	90 nH	Coilcraft Inc. 2222SQ-90NGEB
C_{MR}	95.7 pF	ATC 100B 3R9CW in parallel with ATC 100B 820JW
L_s	360 nH	Coilcraft Inc. 2929SQ-361GEB
C_s	95.7 pF	ATC 100B 5R6CW in parallel with ATC 100B 820JW
C_p	80 pF	ATC 100A 680JW
Switch	$C_{OSS} \sim 118$ pF $R_{ds,ON} \sim 30$ m Ω	EPC 2007

Fig. 14 shows the simulated drain voltage waveforms of the transformed Φ_2 inverter of Fig. 13d for 1x, 2x, 4x, and 10x its rated load resistance R_L of 25 Ω . As can be seen, load modulation by a factor of 10 has only a minor effect on the quasi-trapezoidal drain voltage waveform. It is important to note that the inverter maintains zero-voltage switching despite the modulation of its load.

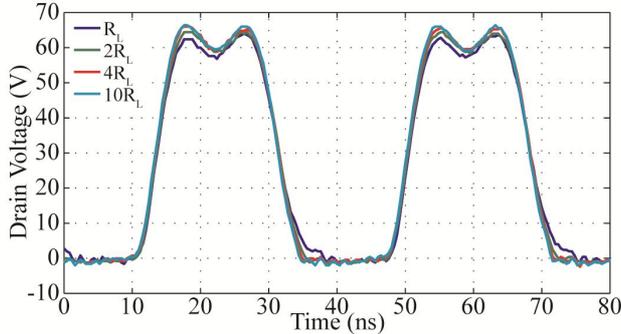


Fig. 14. Drain voltage of the transformed Φ_2 inverter of Fig. 13d for various resistive loads. The rated load resistance is $R_L = 25 \Omega$.

To gain an insight in the operation of the modified inverter, first consider the original design of Fig. 13a. The load voltage is a function of the voltage division formed by R_L and the impedance resulting from L_S and C_S (see Fig. 10). As a result, variation of the load affects the overall phase of the drain impedance, hence altering the characteristics shaping the drain voltage.

In the modified design however, L_S and C_S are in resonance at the converter's switching frequency. Thus, at this frequency only, the inverter's load resistance appears in parallel with its total drain-to-source capacitance (C_{OSS} in parallel with C_P). Thus increasing the load resistance above its rated load value has little effect on the phase or magnitude of Z_{ds} since Z_{ds} is dominated by the drain-to-source capacitance. This is especially true for low inverter loading, in which the load resistance is much larger than the impedance of the drain-to-source capacitance. It can be demonstrated that because of the small impedance (relative to the load) of the drain-to-source capacitance, the drain voltage waveform remains quasi-trapezoidal for much larger load variations than in the case of the traditional Φ_2 inverter.

The measured drain efficiencies (power delivered to the load over dc supply power) versus output power for the traditional (Fig. 13a) and transformed (Fig. 13d) Φ_2 inverter designs are shown in Fig. 15. Gate-driving power losses are excluded. Input power measurements are based on dc input current and voltage measurements using multimeters (34401A, Agilent). An oscilloscope (MSO4054, Tektronix) along with a differential probe (P6251, Tektronix) is used to measure the inverter's output voltage. The output power measurements are based on the oscilloscope-calculated rms output voltage and knowledge of the load resistance (and thus include the harmonic contributions to output power). Each of the employed load resistances is characterized over temperature. Although both inverter designs exhibit similar efficiencies of approximately 90% at rated load, as can be seen from Fig. 15, the transformed inverter design is considerably more efficient with power back-off through load modulation. Of course, lowering the characteristic impedance of all tanks is a way to further reduce the load sensitivity of a Φ_2 design; however, a substantial conduction loss penalty is paid for using

lower-than-necessary characteristic impedance levels, so this approach is not desirable.

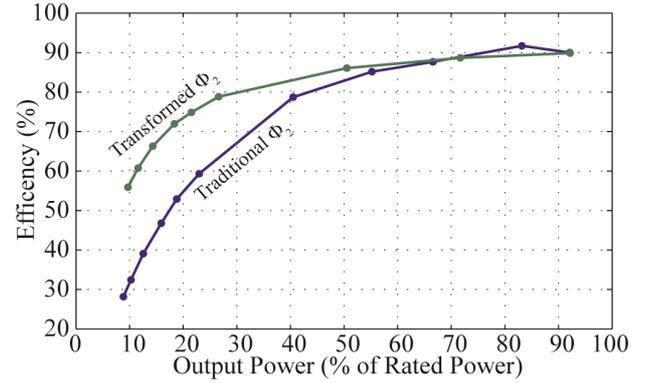


Fig. 15. Drain efficiency for the original and modified Φ_2 inverter designs versus output power through load modulation. The output power axis is normalized to the rated output power for which each inverter is designed.

As a result of the circuit transformations considered above, the quality factor Q of the output series-resonant tank formed by C_S , L_S and R_L may be inadequate for some applications. Even more so, the quality factor will decrease further with increase of the inverter's load resistance. For example, in the Φ_2 inverter considered above (Fig. 13d), the quality factor of the output filter formed by the 96.5 pF capacitor, 357 nH inductor and 25 Ω rated load is only 2.4. However, if the load is increased to 10x the rated load, i.e. $R_L = 250 \Omega$, the quality factor now becomes 0.24. Such a low Q -factor barely provides any filtering of the output. For example, Fig. 17 and Fig. 18 show the measured gate, drain and output voltage waveforms for the transformed Φ_2 inverter design of Fig. 13d with a 25 Ω load and a 250 Ω load respectively. It can be seen that at rated load, the inverter's output is nearly sinusoidal (see Fig. 17), but once the load is increased to 250 Ω , the content of higher harmonics in the inverter's output is obvious (see Fig. 18). In some applications where the load is sensitive to harmonic content, additional filtering must be provided.

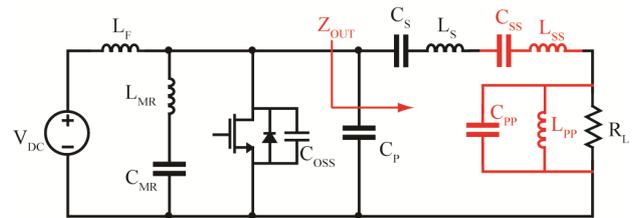


Fig. 16. Augmented schematic of the Φ_2 inverter of Fig. 10 including additional output filtering. The filtering network comprises C_{SS} , L_{SS} , C_{PP} and L_{PP} .

Fortunately, additional filtering can be provided without substantially affecting the inverter's performance. For example, Fig. 16 shows an augmented version of the Φ_2 inverter including an additional series and parallel resonant tank. Note that values of the output filter components are selected so that $L_{SS}C_{SS}$ and $L_{PP}C_{PP}$ are series-resonant and parallel-resonant respectively at the inverter's switching frequency. The series-resonant branch provides most of the filtering at high inverter loading (small load resistance), while the parallel-resonant branch provides most of the filtering at low inverter loading (high load resistance). Other filtering configurations may be implemented, provided that the

impedance Z_{OUT} (see Fig. 16) remains resistive at the inverter's switching frequency over the load modulation range.

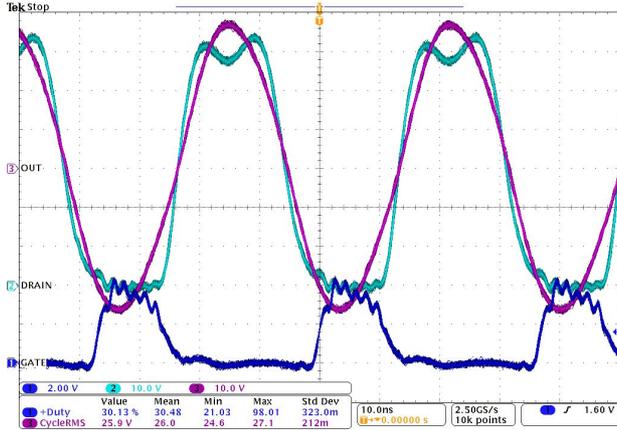


Fig. 17. Gate, drain and load voltage for the transformed Φ_2 inverter of Fig. 13d with $L_F = 68\text{ nH}$, $L_{MR} = 90\text{ nH}$, $C_{MR} = 95.7\text{ pF}$, $C_P = 80\text{ pF}$, $C_S = 95.7\text{ pF}$, $L_S = 360\text{ nH}$, and $V_{DC} = 30\text{ V}$ for rated load R_L of $25\ \Omega$.

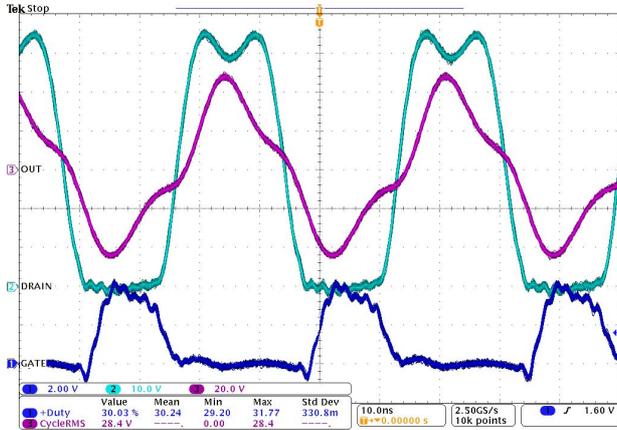


Fig. 18. Gate, drain and load voltage for the transformed Φ_2 inverter of Fig. 13d with $L_F = 68\text{ nH}$, $L_{MR} = 90\text{ nH}$, $C_{MR} = 95.7\text{ pF}$, $C_P = 80\text{ pF}$, $C_S = 95.7\text{ pF}$, $L_S = 360\text{ nH}$, and $V_{DC} = 30\text{ V}$ for 10x the rated load R_L of $250\ \Omega$.

VII. CONCLUSION

This paper presents a methodology for synthesizing single-switch resonant inverters such as Class E inverters for operation at fixed frequency with variable load resistance (i.e., with load modulation). We present a design methodology yielding class E inverter designs that are effective across a wide load resistance range. We focus on identifying the resonant frequencies and characteristic impedances of the key resonant networks in the circuit, and provide guidance of how circuit performance is modified by adjusting these parameters. The efficacy of this approach is demonstrated in both simulation and in an experimental prototype inverter at 27.12 MHz. The inverter design developed using this approach has been successfully employed for load modulation operation in a multi-way outphasing power amplifier system [36, 37]. We also show how this design methodology relates to circuit transformations on classical class E designs, and demonstrate how the transformation-based approach can also be employed to reconfigure designs with higher-order tunings for variable-resistance operation. It is expected that the presented work will be widely useful in applications where single-switch inverters are operated under

variable-resistance-load operation, such as in dc-dc converters and outphasing power amplifiers.

VIII. APPENDIX I

Section II outlined a simple methodology for designing a class E inverter that maintains ZVS over a wide load modulation range. This Appendix provides a discussion of the theory for selecting the input network of the inverter formed by components L_F and C_F (see Fig. 1). Here we present a derivation of the input tank resonant frequency necessary for ensuring ZVS across load modulation, and we explain the proposed frequency tuning range proposed in Section II. Furthermore, we demonstrate that in order to guarantee ZVS across the full load range, it is necessary to tune the inverter's output network (L_S , C_S , L_P , C_P , see Fig. 1) to be resonant at the inverter's switching frequency. Finally, we provide guidelines on selecting the input network characteristic impedance, and we discuss its effects on the inverter's performance.

In order to understand the frequency to which the input resonant tank (L_F and C_F) of the class E inverter of Fig. 1 should be tuned to maintain ZVS across a wide load modulation range, first consider an unloaded version of the class E inverter as shown in Fig. 19A. The circuit comprises only the input resonant tank formed by C_F and L_F , a switch S , and a dc supply V_{DC} . For sake of simplicity, assume that L_F and C_F are ideal (no parasitic components) and that the switch S behaves as a short or open circuit when respectively closed or opened. Assume that S is switched with a 50% duty cycle for long enough time to allow the circuit to reach its periodic steady-state operation. Now suppose that at time T_{OFF} (after the circuit has reached steady-state operation) the switch is turned-off as part of its switching cycle and then kept off for the rest of time. The resulting drain voltage waveform is shown in Fig. 19B.

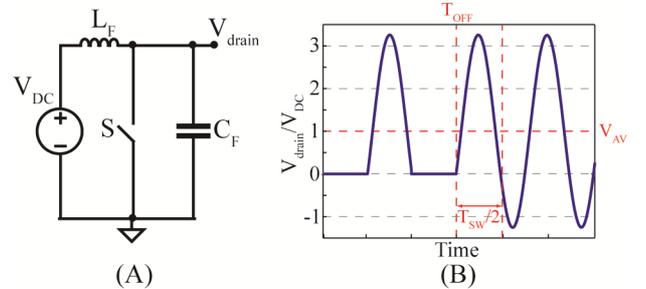


Fig. 19. Schematic of the unloaded class E inverter of Fig. 1 (A), and its simulated drain voltage (B). Prior to T_{OFF} , switch S is switched with 50% duty-cycle, while past T_{OFF} , S is kept off. L_F and C_F are selected to ensure ZVS at no load.

As can be seen from Fig. 19B, the drain voltage continues to resonate at the resonant frequency of L_F and C_F . Note that from steady-state analysis the cycle average of the drain voltage before and after T_{OFF} must be equal to the supply voltage V_{DC} . Furthermore, since we have assumed no losses in the circuit, the oscillations in drain voltage V_{drain} after T_{OFF} are undamped and sinusoidal with some frequency f_{IN} and amplitude A_{IN} . Thus we can express V_{drain} as per (30):

$$V_{drain} = A_{IN} \cos(2\pi f_{IN} t) + V_{DC}. \quad (30)$$

Note that according to the drain voltage representation we have chosen in (30), the peak of the drain voltage corresponds to $t = 0$. This choice simplifies

the mathematical expressions, although the absolute phase of the drain voltage expression is irrelevant to the present discussion, and any other choice will yield identical results.

In order to ensure ZVS at no load, V_{drain} must go from 0 V to its peak amplitude and then back to 0V in half of a switch period T_{SW} (see Fig. 19B). In reference to (30), this can be rewritten according to (31):

$$V_{drain}\Big|_{\frac{T_{SW}}{4}} = A_{IN} \cos\left(2\pi f_{IN} \frac{T_{SW}}{4}\right) + V_{DC} = 0. \quad (31)$$

Furthermore, the positive portions of V_{drain} before and after T_{OFF} are identical, and hence, the cycle average of V_{drain} prior to T_{OFF} can be expressed by (32):

$$\int_{-T_{SW}/4}^{T_{SW}/4} (A_{IN} \cos(2\pi f_{IN} t) + V_{DC}) dt = V_{DC} T_{SW}. \quad (32)$$

Solving (31) and (32) simultaneously for f_{IN} and A_{IN} yields (33) and (34) respectively:

$$f_{IN} \approx 1.29 f_{SW} \quad (33)$$

$$A_{IN} \approx 2.27 V_{DC}, \quad (34)$$

where f_{SW} is the switching frequency of the inverter, $f_{SW} = 1/T_{SW}$. Thus, to ensure ZVS at no load, we can conclude from (33) that the inverter's input network must be tuned for resonance at a frequency that is approximately 30% higher than the inverter's switching frequency.

It is interesting and instructive to consider what happens to the operation of the inverter of Fig. 19A when its drain is loaded. Fig. 20 shows the inverter of Fig. 19 with a loading current source I_L connected to its drain node. Suppose that the load current is a pure sinusoid with a frequency equal to the inverter's switching frequency f_{SW} , amplitude $|I_L|$ and such a phase so that the load current waveform is in phase with the drain voltage, i.e. I_L is positive when the switch is off, and I_L is negative when the switch is on (see Fig. 20B). Assume for the present discussion that the switch is operated at 50 % duty cycle. We can then express I_L by (35):

$$I_L = |I_L| \sin(2\pi f_{SW} t). \quad (35)$$

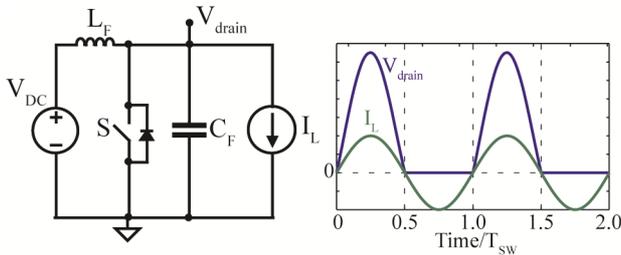


Fig. 20. Schematic of a loaded class E inverter of Fig. 1 (A), and an example of its drain voltage waveform for a relatively small loading current magnitude $|I_L|$ (B). The inverter load current I_L is sinusoidal with a frequency equal to the inverter's switching frequency and in phase with the drain voltage.

Again, the absolute phase of I_L is irrelevant as long as the load current is in phase with the drain voltage waveform. Let us now investigate the effect of I_L on the drain crossover voltage V_X , i.e. the drain voltage value at the moment the switch S is turned-on. Note that a non-

zero V_X suggests that the C_F capacitor stores some residual charge right before switch turn-on which is lost once the switch is turned on, thus giving rise to switching losses. Indeed, this indicates non-ZVS inverter operation.

By employing linear circuit analysis, it can be shown that the drain voltage V_{off} during the switch off-period is given by (36):

$$V_{off} = V_{DC} (1 - \cos(2\pi f_{IN} t)) + i_0 \sqrt{\frac{L_F}{C_F}} \sin(2\pi f_{IN} t) - |I_L| \sqrt{\frac{L_F}{C_F}} \frac{\cos(2\pi f_{IN} t) - \cos(2\pi f_{SW} t)}{(f_{SW}/f_{IN} - f_{IN}/f_{SW})} \quad (36)$$

where f_{IN} is the resonant frequency of L_F and C_F , f_{SW} is the inverter's switching frequency, $|I_L|$ is the amplitude of the load current, and i_0 is the initial current in the L_F inductor at the moment the switch is turned off. Note that (36) is only valid during the period when the switch is off and only once the circuit has reached steady-state operation. For sake of simplicity of the expressions, we define $t = 0$ to be the moment at which the switch is turned off and the drain voltage is allowed to ring. Thus in (36), V_{off} is defined only for $0 \leq t \leq T_{SW}/2$.

Furthermore, it can be shown that the initial current i_0 in the L_F inductor at switch turn-off can be expressed in terms of the supply voltage V_{DC} and the load current amplitude $|I_L|$:

$$i_0 = V_{DC} \sqrt{\frac{C_F}{L_F}} \frac{\sin(\pi k) + \pi k}{1 - \cos(\pi k)} + |I_L| \frac{k \sin(\pi k)}{(1 - k^2)(1 - \cos(\pi k))} \quad (37)$$

where k is the ratio of f_{IN} to f_{SW} , i.e. $k = f_{IN}/f_{SW}$. As we shortly demonstrate, to ensure ZVS operation across load modulation, k must be selected according to (33). Note that by substituting (37) into (36) and evaluating V_{off} at $t = T_{SW}/2$, one can obtain the crossover voltage V_X (the drain voltage at switch turn-on) in terms of the inverter's supply voltage and the load current magnitude. Through algebraic manipulations, it can be shown that irrelevant of the load current magnitude $|I_L|$, the drain voltage is always zero at switch turn-on ($V_X = 0$), provided that the load current is purely sinusoidal and in phase with the drain voltage (see Fig. 19B), and L_F and C_F are resonant at f_{IN} as per (33). Thus we can conclude that as long as the loading current is purely sinusoidal and in phase with the drain voltage, the inverter will exhibit ZVS for any load.

In reality, however, one does not have direct control of the phase or waveform shape of the inverter's load current. Instead, it is determined by the drain voltage waveform and the characteristic of the load impedance. Consider again the loaded class E inverter of Fig. 20A. Fig. 20B shows the drain voltage waveform shape for no load ($|I_L| = 0$), or for relatively small load current magnitudes $|I_L|$ compared to the inverter's maximum rated loading. For such low-loading conditions, it can be shown by reference to (37) and (36) that the drain voltage waveform during the switch off-period is symmetrical about $t = T_{SW}/4$. An important property of the drain voltage waveform at low current loading is that its first harmonic is in phase with the drain voltage. In other words, if we were to plot the first harmonic (at the switching frequency) of the drain voltage at low-loading conditions, it will be entirely positive during the switch off-period and entirely negative during the switch on-

period. Thus if we terminate the inverter's output with an impedance network that is purely resistive at the switching frequency f_{SW} while attenuating higher harmonic frequencies, then the resulting load current can be nearly sinusoidal at the switching frequency and in phase with the drain voltage. This is indeed the reason for tuning the series ($L_S C_S$) and parallel ($L_P C_P$) tanks in Fig. 1 to resonance at the inverter's switching frequency.

As long as the inverter's load current is sinusoidal and aligned with the drain voltage, the inverter is guaranteed to operate in ZVS mode and hence reduce switching losses. However, increasing the inverter's load current distorts the drain voltage waveform from the one shown in Fig. 20B, causing a certain time-shift between the drain voltage and its fundamental component. This in turn results in a change in alignment between the loading current and the drain voltage, hence leading to loss of ZVS. The degree to which higher loading currents affect the drain voltage waveform and its effect on ZVS depends on the characteristic impedance of the input network (L_F and C_F in Fig. 1) relative to the inverter's rated load (minimum loading impedance).

Higher characteristic impedances of the input-side network result in larger distortions of the drain voltage waveform with increase of loading current, leading to bigger misalignment between the load current and the drain voltage and ultimately yielding an increase in the switching losses. Conversely, smaller characteristic impedances result in larger circulating reactive currents in the input network. As a consequence, increasing the inverter's loading current has less effect on the drain voltage waveform and causes less change in alignment between the loading current and the drain voltage. As a result, the inverter is able to maintain ZVS over a wider load modulation range. The latter benefit however is at the expense of larger power losses at the input network due to the higher circulating currents.

The effect of the characteristic impedance of the $L_F C_F$ input network (see Fig. 1) on the ability of the inverter to maintain ZVS across load modulation is clearly shown in Fig. 21. Fig. 21 is obtained by simulating the class E inverter of Fig. 1 and measuring the crossover voltage V_X (the drain voltage at the moment the switch is turned-on) at different inverter loads for a range of input network resonant frequencies f_{IN} . Plots for four different characteristic impedances of the $L_F C_F$ input network are shown. k_f is the ratio of the inverter's rated load R_{min} to the input tank characteristic impedance as given by (4). Note that Fig. 21 is generated for a class E inverter with only a series-resonant output tank with a quality factor of $Q = 10$ (the parallel $L_P C_P$ tank in Fig. 1 is not included). Furthermore, the body diode of the transistor is also ignored in the simulation.

As can be seen from Fig. 21, as the inverter's loading resistance is increased, the inverter's loading current decreases, and it exhibits ZVS operation ($V_X = 0$) at an input network resonant frequency $f_{IN} \approx 1.29f_{SW}$ irrespective of the characteristic impedance of the input tank. This is indeed the frequency derived from (31) and (32) and given by (33) for the low-loaded operation of a class E inverter. Furthermore, one can see from Fig. 21 that as input network characteristic impedance decreases, the variation of the necessary f_{IN} for ZVS with loading also decreases. As described earlier, this is because the lower characteristic impedance results in higher circulating currents in the input network, and so variation of the inverter's loading current has less effect on its drain

voltage waveform. For example, for $k_f = 0.2$ (see Fig. 21), the f_{IN} necessary for maintaining ZVS across a 10:1 load modulation is approximately as given by (33) for the low-loaded inverter operation.

On the other hand, as can be seen from Fig. 21 ($k_f = 1.25$ and $k_f = 1.0$), increasing the input network characteristic impedance results in larger variations of the necessary f_{IN} to maintain ZVS with load modulation. For example, for $k_f = 1.25$, to ensure ZVS operation at rated load, the input tank must be tuned to resonance at approximately 1.5 times the inverter's switching frequency. In this case however, once the inverter's loading decreases significantly (load resistance increases), the inverter will lose ZVS and the drain voltage at the moment the switch is turned-on will be negative. Note that in reality however, the drain voltage is clamped via the transistor's body diode, so negative drain voltages are limited to the diode's forward voltage drop. Thus even for the above case ($k_f = 1.25$ and $f_{IN} = 1.5f_{SW}$), at light loads, the inverter will still exhibit nearly ZVS operation. This explains why Section II proposes a frequency range of $1.3f_{SW}$ to $1.5f_{SW}$ for f_{IN} .

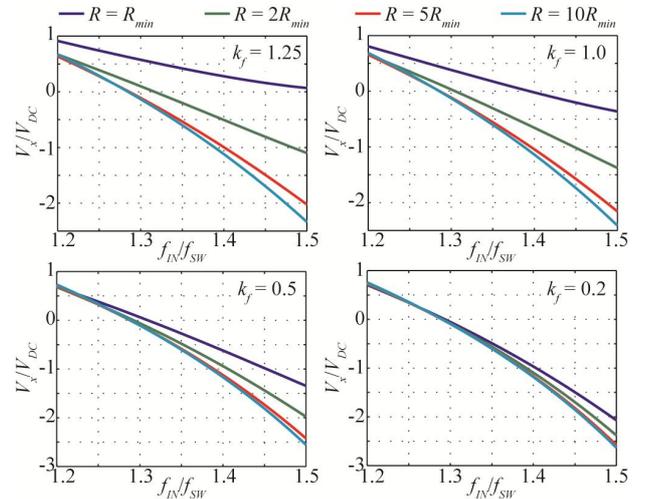


Fig. 21. Normalized crossover voltage V_X versus normalized input tank resonant frequency f_{IN} for 1x, 2x, 5x, and 10x the rated inverter load (R_{min}) and for various input tank characteristic impedances ($k_f = \sqrt{L_F / C_F} / R_{min}$) for the class E inverter of Fig. 1.

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