

©2000 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.

Room-Temperature Testing for High Critical-Current-Density Josephson Junctions

Michael J. O'Hara and Karl K. Berggren

Abstract—This paper demonstrates that room-temperature resistance measurements can accurately predict the critical current and normal resistance of high critical-current-density junctions. We fabricated high critical-current-density ($\sim 200 \mu\text{A}/\mu\text{m}^2 = 20 \text{ kA}/\text{cm}^2$) Nb/Al/AIO_x/Nb Josephson junctions in cross-bridge Kelvin resistor (CBKR) test structures and measured their electrical characteristics both at 4.2 K and at room temperature. We developed a two-dimensional mathematical model of the CBKR test structure with two resistive wiring layers in order to characterize the effect of current crowding on the room-temperature measurements. We then used the model to remove the effect of current crowding from the room-temperature measurements and correlated the values of these measurements to the electrical properties of the junctions at 4.2 K. We also identified test-structure-design rules that guarantee current crowding is negligible.

Index Terms—Cross-bridge Kelvin resistors, high critical-current-density, Josephson junctions, room-temperature testing, test structures, tunneling resistance.

I. INTRODUCTION

THE critical current I_c and normal resistance R_n of Nb/Al/AIO_x/Nb Josephson junctions can be predicted with a room-temperature measurement [1]. This was demonstrated previously for junctions with a relatively low critical-current density J_c of $17 \mu\text{A}/\mu\text{m}^2$. However, the $I_c R_n$ product should depend only on the gap voltage and the temperature, so we should be able to use this relationship on high- J_c junctions even though they have some different processing and electrical characteristics. This paper demonstrates that the I_c and R_n of high- J_c ($\sim 200 \mu\text{A}/\mu\text{m}^2$) junctions can also be predicted by using a room-temperature measurement.

It is important for the large-scale manufacturability of Josephson junctions to be able to measure their critical currents and normal resistances quickly and cheaply. Low-temperature testing is time consuming: each of the dozens of chips from every wafer must be carefully mounted onto a probe and loaded into a liquid-helium dewar, and the number of measurements is limited by available signal pads to a few test structures per chip. Moreover, it is difficult to probe a wafer at low temperature without dicing it, thus the wafers cannot

Manuscript received May 26, 2000; revised December 5, 2000. This work was supported by the Lincoln Laboratory Advanced Concepts Program. The Advanced Concepts Program is supported principally by the Department of the Air Force under Contract F19628-00-C-0002.

The authors are with the MIT Lincoln Laboratory, Lexington, MA 02420-9108 USA.

Publisher Item Identifier S 1051-8223(00)11736-1.

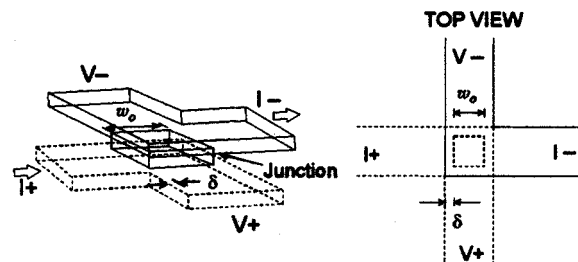


Fig. 1. Schematic diagram of a CBKR test structure. Current flows in through I+ in the bottom electrode, through the barrier, and out through the top electrode (I-). Potential is measured on either side of the barrier using the V+ and V- leads.

be tested until processing has been completed. On the other hand, four-point room-temperature measurements can be made automatically on all test structures across an entire wafer, using commercial test equipment. Thus the wafers can be measured during processing: to determine the electrical properties of the junctions, one simply has to load the wafer into an automated probe station and wait.

The resistance of a junction can be measured with a simple cross-bridge kelvin resistor (CBKR) test structure [2] consisting of a Josephson junction with four leads, two on each side of the junction, as shown in Fig. 1. Current is passed in the I+ lead, through the junction, and out the I- lead on the opposite side of the junction. Since the V+ and V- leads are orthogonal to the flow of current, they provide a good estimate of the potential on either side of the junction. The resistance of the junction can be calculated by dividing the potential difference between the V+ and V- leads by the current from the I+ to I- lead. Without such a four-point measurement the lead resistance would be impossible to distinguish from the resistance of the contact.

The voltage measured on the V+ and V- leads of a CBKR test structure does not perfectly represent the potential on either side of the junction. The imperfection is due to an effect known as current crowding, in which current deviates from a direct path through the junction and is free to enter the junction from all sides, like water in a bathtub entering the drain. The measured resistance of the test structures is higher than that of the junction because some of the resistance of the leads is also being measured. Fig. 2 shows the inhomogeneous current distribution through one layer of a test structure as calculated using the model described in this paper.

In the semiconductor industry similar structures are used to determine the contact resistance between metal wiring

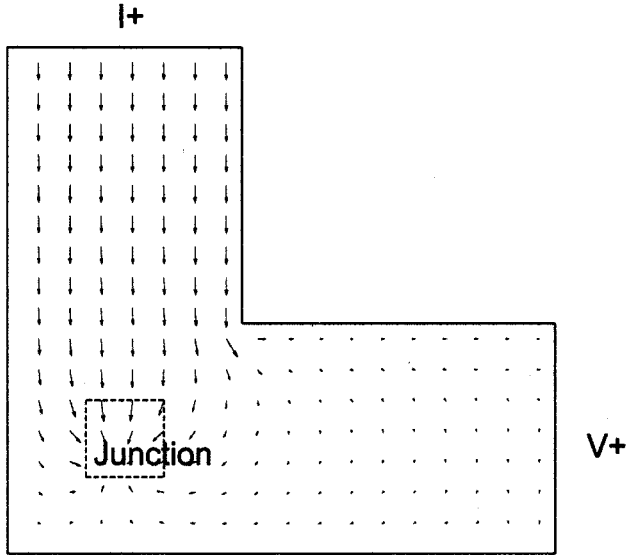


Fig. 2. Vector plot of the current flow through one of the electrodes of a CBKR test structure. Current flows in through the current source at one end of the electrode and out the junction. Note that the current not only flows linearly into the junction, but also around the junction, creating a small potential drop from the junction to V_+ . The sheet resistances of the two layers used in the calculation are $0.906 \Omega/\square$ and $2.12 \Omega/\square$, and the specific contact resistivity was $150 \Omega/\mu\text{m}^2$. The lead margin was set to be particularly large in order to allow easy visualization of the current-crowding effect.

layers and semiconducting device layers. The effects of current crowding in these contacts have been well studied [3]. However, the results obtained from research on metal-semiconductor contacts are not directly applicable to CBKR test structures for Josephson junctions because, in the case of metal-semiconductor contacts, the metal layer may be assumed to have negligible resistance relative to the semiconductor layer, whereas in the Josephson-junction test structures the wiring layers have approximately equal resistance.

We developed a mathematical model of the test structure in two dimensions and solved it numerically to calculate the error from current crowding. We then manufactured CBKR test structures with high- J_c Josephson junctions. We measured the resistance of the junctions at room temperature and their electrical properties at 4.2 K. We corrected the room-temperature measurements using the model and correlated the results to the electrical properties of the junctions at 4.2 K.

II. MODELING THE TEST STRUCTURE

A. Governing Equations

The CBKR test structure can be accurately modeled using classical theory. The flow of current in a conductor with no free charge is governed by the Laplace equation

$$\nabla^2 V = \frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} + \frac{\partial^2 V}{\partial z^2} = 0. \quad (1)$$

We establish the boundary conditions as follows: the edge of the current source is fixed, while the current drain is grounded. We also need boundary conditions for the remaining edges of the test structure. Since current flows through the electrodes but not out the sides, we can set the normal current equal to zero at

the sides of the conductor. We can also fix a positive potential at I_+ (see Fig. 1) and ground I_- .

This equation with associated boundary conditions is sufficient to model the potential distribution in three dimensions and to extract numerically the current from I_+ to I_- and the potential difference from V_+ to V_- . However, we can reduce the computational requirements of this model by flattening it to two dimensions. This approximation is very good because the potential drop in the z -direction has a negligible effect on the V_+ and V_- potential for our test structure dimensions and resistivities [3]. However, in the case of very small contact resistance, large sheet resistance, thick wiring layers, and small junctions, the third dimension would become significant.

B. Reduction to Two Dimensions

To reduce the model to two dimensions, we make some assumptions [3]. Each metal layer is treated as a separate two-dimensional plane. In the area not directly above or below the junction, current does not flow up or down out of the leads. Thus we eliminate the z term in (1), so for convenience we introduce a new operator $\nabla_t^2 = \partial^2/\partial x^2 + \partial^2/\partial y^2$ that differs from ∇^2 only in that it is not dependent on z . In the area of the lead not directly over the junction, (1) reduces to

$$\nabla_t^2 V = \frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} = 0. \quad (2)$$

In the areas directly over and under the junction, current flows out of one layer into the other, so the two-dimensional divergence of current in each layer is nonzero. Thus we must return to the three-dimensional equation. We rewrite (1) with the new operator ∇_t^2 , and substitute $\partial^2 V/\partial z^2$ with $-\sigma^{-1} \cdot \partial J_z/\partial z$, to get

$$-\sigma \nabla_t^2 V + \frac{\partial J_z}{\partial z} = 0$$

where σ is the film conductivity and J_z is the current density in the z direction. We now integrate along the z -axis from the top of the top layer ($z = z_0$) to the junction interface ($z = 0$). We assume $\nabla_t^2 V$ is constant with respect to z , and we let R_s be the sheet resistance of the layer under consideration. Thus we find

$$-R_s^{-1} \nabla_t^2 V + J_z(z_0) - J_z(0) = 0.$$

From our three-dimensional boundary conditions, $J_z(z_0) = 0$. Here $J_z(0)$ is the vertical current density through the junction, which is the potential difference across the junction divided by the contact resistivity. Thus if we let V_1 be the potential immediately above the junction, V_2 be the potential immediately below the junction, and ρ_c be the specific contact resistivity, we get

$$-R_s^{-1} \nabla_t^2 V + \frac{V_1 - V_2}{\rho_c} = 0. \quad (3)$$

We can use (2) and (3) to describe any point on the interior of the electrodes. We fix the potential at the end of one electrode and ground the opposite end on the other electrode. For the other edges, we can simplify (2) with the assumption that current does not flow out the edges of the electrodes.

C. Solving the Boundary Value Problem

Two-dimensional boundary value problems of this type can be solved by first discretizing the test structure area into sample points and then applying a numerical relaxation technique. The differential equations in the problem are solved on a discrete grid. The relaxation technique can be described as follows.

First we make a simple initial guess at the potential distribution in the leads. Then, for each point, we adjust its value so that it satisfies the equations relating it to its neighboring points. After the value at each point has been adjusted, the new set of points is closer to the solution than the initial guess. We repeat this procedure until the values of the points satisfy the equations relating them to each other to within a given tolerance. If we assume that the calculated adjustment will not be sufficient, because the neighboring points themselves will be adjusted in the next iteration, we can overadjust. This procedure is called successive overrelaxation [4] and greatly accelerates convergence.

D. Extracting Measurable Quantities

Once potential as a function of position has been solved for, the potential difference one would measure with the voltage leads is simply the difference of the average potential values at the ends of the V+ and V- leads. In order to solve for current, we return to $J = -\sigma \nabla V$ and choose a cross-sectional area integral of J such that all current passes through that cross section. In our two-dimensional model, this cross-sectional integral is a line integral across one of the current leads, or an area integral across the junction.

The technique as described thus far takes ρ_c as an input and gives the measured $V/I = R_k$, the contact resistance. However, in practice one measures an experimental value R_k and wants to know ρ_c . To find ρ_c , we iterate the model while varying ρ_c until a ρ_c input that returns the measured R_k is found. For an initial guess, we take $\rho_c = R_k \cdot w_0^2$, where w_0 is the length of the junction on a side. This value of ρ_c would be the solution in the case of no current crowding. Then, we model the structure to see how close the output R is to R_k . If they disagree, we multiply ρ_c by R_k/R and repeat until the result converges. For our typical test structures, convergence to less than 1% usually requires only a few iterations.

E. Generalized Result

It is useful for a designer to determine the error due to current crowding without having to perform simulations. Thus we generalized the results of the model. There are five inputs, the physical dimension δ (defined in Fig. 1), w_0 , R_k , and the sheet resistance of the two electrodes R_{s1} and R_{s2} , and one output ρ_c , so it is difficult to represent the results graphically. However, by running the model for a matrix of these parameters, we identified rules that guarantee negligible current crowding. The rules are a straightforward extension of the one-resistive-electrode case [3] and simply require that $w_0 \gg \delta$, and $R_k \gg R_{s1}$, and $R_k \gg R_{s2}$.

For the junctions we fabricated, $w_0/\delta \approx 3$, and $R_k/R_{s1} \approx 15$, and $R_k/R_{s2} \approx 7$. The model shows that the zero-dimensional model is a good approximation with these parameters,

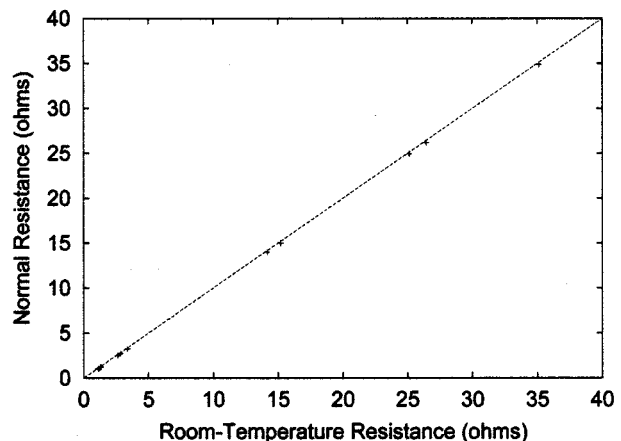


Fig. 3. Plot of the normal resistance R_n of junctions measured at 4.2 K versus the junction resistance R_k of the test structures measured at 300 K. The line is the identity mapping.

and in fact the two-dimensional model provides only a $\sim 2\%$ correction.

III. EXPERIMENTAL RESULTS

CBKR test structures were fabricated on a 150-mm-diameter wafer using an abbreviated version¹ of the Lincoln Laboratory DPARTS (doubly-planarized all-refractory technology for superconductors) process [5]. The junctions were made of Nb/Al/AIO_x/Nb trilayers and had critical current densities of 200 $\mu\text{A}/\mu\text{m}^2$ (20 kA/cm²). All the test structures were measured at room temperature using a Rucker & Kolls 683A Semi-Automatic Wafer Prober with a Hewlett-Packard 3478A Multimeter. The finite-element analysis model was used to determine ρ_c from the measured resistances. Then the wafers were diced, and junction I-V curves were measured of 11 junctions at 4.2 K in liquid helium. The I-V curves were recorded digitally, and a computer program extracted parameters including critical current I_c and normal resistance R_n . We then looked for correlations between the room-temperature and 4.2-K results.

In Fig. 3, R_n is plotted versus room-temperature junction resistance R_k . The model was used to correct the values, resulting in a small improvement in the linear fit. The identity mapping provides a close approximation to these results, as seen in Fig. 3. The RMS deviation of the actual normal resistance from the predicted normal resistance is 0.14 Ω , and the correlation coefficient is 0.9995. This result can be used to accurately predict the normal resistance of high- J_c junctions at 4.2 K with a room-temperature measurement.

I_c is plotted versus the corrected room-temperature resistance in Fig. 4. Here, the RMS deviation of the actual value from the predicted is 58 μA for the junctions, which range in critical current from 32 μA to 1992 μA . The Pearson's correlation coefficient is 0.9974. The slope of the least squares fit is 1.9 mV = 0.68 V_g , where V_g is the gap voltage of niobium (about 2.85 mV)². When a linear fit is performed on the five smallest junctions

¹The layer of niobium acting as a ground plane and the corresponding layer of insulation oxide are not necessary for the fabrication of test structures. Thus those layers were omitted in order to save processing time and cost.

²This is the same value a similar analysis [1] of low- J_c junctions yields, as one should expect.

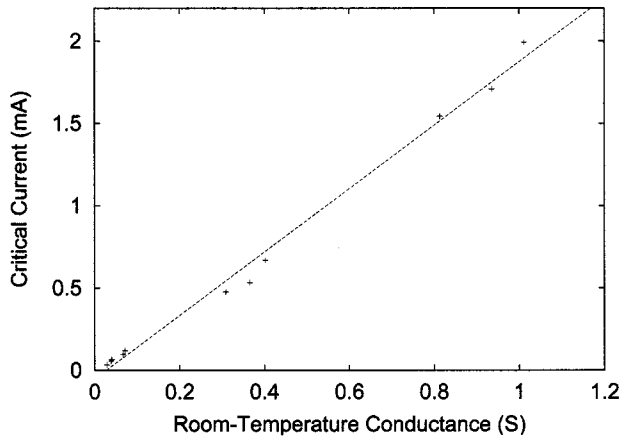


Fig. 4. Plot of the critical current I_c of junctions measured at 4.2 K versus the inverse of the junction resistance, $1/R_k$, of the test structures measured at 300 K. The slope of the linear fit is 1.9 mV, which is $0.68 \cdot V_G$ and corresponds to experimental results for low- J_c junctions.

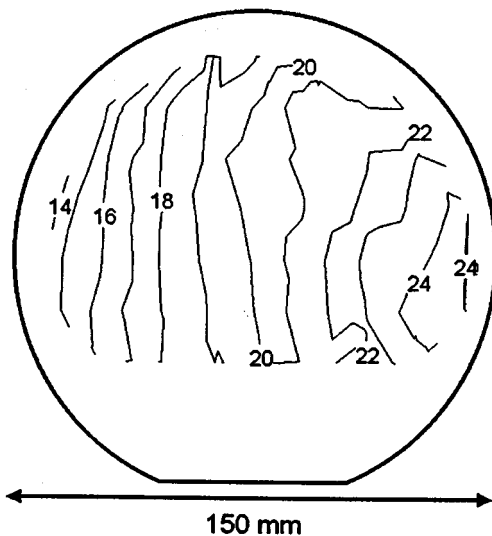


Fig. 5. Wafer map of J_c in kA/cm^2 extracted from room-temperature resistance measurements. There is variation from the left to the right of the wafer of about 20% of the mean.

tions, ranging in critical current from $32 \mu\text{A}$ to $120 \mu\text{A}$, the RMS deviation is only $6.1 \mu\text{A}$. Thus we can accurately predict the critical current of high- J_c junctions with a room-temperature measurement.

Using this correlation between critical current and room-temperature resistance for several dice on the wafer, we can calculate critical current density on the rest of the dice measured only

at room temperature. The wafer map of J_c for this experiment is shown in Fig. 5. The majority of the critical currents lie within 90% and 120% of the targeted critical-current density. The pattern and detail evident in this map have provided us with important clues in determining the source of cross-wafer J_c variation.

IV. CONCLUSION

We have developed a model of room-temperature Josephson-junction test structures to more accurately extract critical currents. We have also demonstrated that room-temperature test structures may be used to determine the critical current of high-critical-current-density Josephson junctions. Using the room-temperature measurement technique, we can create wafer maps of J_c for entire lots of wafers.

Finally, we have presented a general framework that can be used to design test structures of this type with low inherent measurement error.

ACKNOWLEDGMENT

Opinions, interpretations, conclusions, and recommendations are those of the author and are not necessarily endorsed by the United States Air Force. The authors would like to thank G. Sollner, J. Sage, D. Feld, A. H. Worsham, and R. Patt for helpful comments and discussion, T. Weir and G. Fitch for help with testing, and D. Baker and E. Macedo for help with fabrication.

REFERENCES

- [1] K. K. Berggren, M. O'Hara, J. P. Sage, and A. H. Worsham, "Evaluation of critical current density of Nb/Al/AIO_x/Nb Josephson junctions using test structures at 300 K," *IEEE Trans. Applied Superconduct.*, vol. 9, pp. 3236–3239, June 1999.
- [2] S. J. Proctor, L. W. Linholm, and J. A. Mazer, "Direct measurements of interfacial contact resistance, end contact resistance, and interfacial contact layer uniformity," *IEEE Trans. Electron. Devices*, vol. ED-30, pp. 1535–1542, Nov. 1983.
- [3] W. M. Loh, S. E. Swirhun, T. A. Schreyer, R. M. Swanson, and K. C. Saraswat, "Modeling and measurement of contact resistances," *IEEE Trans. Electron. Devices*, vol. ED-34, pp. 512–524, Mar. 1987.
- [4] W. H. Press, S. A. Teukolsky, W. T. Vetterling, and B. P. Flannery, *Numerical Recipes in C*. Cambridge, U.K.: Cambridge Univ. Press, 1992.
- [5] K. K. Berggren, E. M. Macedo, D. A. Feld, and J. P. Sage, "Low T_c superconductive circuits fabricated on 150-mm-diameter wafers using a doubly planarized Nb/AIO_x/Nb process," *IEEE Trans. Applied Superconduct.*, vol. 9, pp. 3271–3274, June 1999.

Michael J. O'Hara, photo and biography not available at the time of publication.

Karl K. Berggren, photo and biography not available at the time of publication.